Lesson Plan

Discipline : Computer Engg.
Semester : 3rd
Subject : DigitalElectronics
LessonPlanDuration: 16 weeks
Workload(Lecture/Practical)perweek(inhours):Lectures—03,Practical—03

Week	Theory		Practical	
	Lecture Day	Topic(IncludingAssignment/Test	Practical Day	Topic
1st	1	Introduction	1st	Verification and interpretationof truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and ExclusiveNOR (EXNOR)gates
	2	Distinctionbetweenanalogganddigital signal.		
	3	Applicationsandadvantagesofdigital signals		
2nd	4	Assignment	2nd	Verification and interpretationof truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and ExclusiveNOR (EXNOR)gates
	5	Binary		
	6	octalandhexadecimalnumbersystem		
3rd	7	conversion from decimal and hexadecimaltobinaryandvice-versa	3rd	Realisationoflogic functions with the help of NAND or NOR gates
	8	Binary addition and subtraction includingbinarypoints.1'sand2's complement method of addition/subtraction.		
	9	Assignment		
4th	10	Conceptofcode,weightedandnoweighted codes	4th	To design a half adder using XOR and NAND gates andverificationof its operation
	11	examplesof8421,BCD,excess-3and Gray code		
	12	Conceptofparity,singleanddouble parity and error detection		
5th	13	Assignment	5th	Constructionofa fulladdercircuit
	14	Conceptofnegativeandpositivelogic		

	15	Definition,symbolsandtruthtablesof NOT,AND,OR,NAND,NOR,EXORGates		using XOR and NANDgatesand verify its operation
6th	16	NANDandNORasuniversalgates	6th	Revision of Experiments
	17	IntroductiontoTTLandCMOSlogic families		
	18	Assignment		
7th	19	LogicSimplification	7th	Revision of Experiments
	20	Postulates of Boolean algebra, De Morgan's Theorems		
	21	Implementation of Boolean (logic) equation with gates		
8th	22	Assignment	8th	Verificationoftruth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one ICeachofDlatch,D flip-flop,JKflip-flops).
	23	HalfadderandFulladdercircuit		
	24	designandimplementation		
9th	25	Decoders, Multiplexers, Multiplexers and Encoder	9th	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops(AtleastoneIC each of D latch, D flip-flop, JK flip-flops).
	26	Four bit decoder circuits for 7 segment display and decoder/driver ICs		
	27	Basicfunctionsandblockdiagramof MUX and DEMUX with different ICs		
10th	28	Basicfunctionsandblockdiagramof Encoder	10th	Revision of Experiments
	29	Assignment		
	30	Conceptandtypesoflatchwiththeir working and applications		
11th	31	Operationusingwaveformsandtruth tablesofRS,T,D,Master/SlaveJKflip flops	11th	Verificationoftruth table for encoder and decoder ICs, Mux and DeMux
	32	Differencebetweenalatchandaflip flop		
	33	Introduction to Asynchronous and Synchronouscounters		

12th	34	Binarycounters	12th	Todesigna4bit SISO,SIPO,PISO, PIPO shiftregisters usingJK/Dflipflops and verification of their operation
	35	DividebyNripplecounters		
	36	Decade counter		
13th	37	Ringcounter	13th	Revision of Experiments
	38	Assignment		
	39	Introduction and basic concepts including shift left and shift right		
14th	40	serialinserialout,parallelinserialout parallel in parallel out parallelin parallel out Universal shift register	14th	To design a 4 bit ring counter and verifyitsoperation.
	41	WorkingprincipleofA/DandD/A converters		
	42	StairstepRampA/Dconverter,Dual SlopeA/Dconverter		
15th	43	Successive Approximation A/D Converter	15th	Use of Asynchronous CounterICs(7490 or7493)
	44	BinaryWeightedD/Aconverter		
	45	R/2R ladder D/A converter, Applications of A/D and D/A converter		
16th	46	Memoryorganization,classificationof semiconductormemories(RAM,ROM, PROM, EPROM, and EEPROM)	16th	Revision of Experiments
	47	staticanddynamicRAM		
	48	introductionto74181ALUIC		