8085 Microprocessor Architecture & Working

- ELECTRONICS
  0 COMMENT

Generally, the 8085 is an 8-bit microprocessor, and it was launched by Intel team in the year of 1976 with the help of NMOS technology. This processor is the updated version of the microprocessor. The configurations of 8085 microprocessor mainly include data bus-8-bit, address bus-16 bit, **program counter**-16-bit, stack pointer-16 bit, registers 8-bit, +5V voltage supply and works at 3.2 MHz single segment CLK. The applications of 8085 microprocessor include microwave ovens, washing machines, gadgets, etc. This article discusses an overview of what is 8085 microprocessor architecture.

8085 Microprocessor Architecture

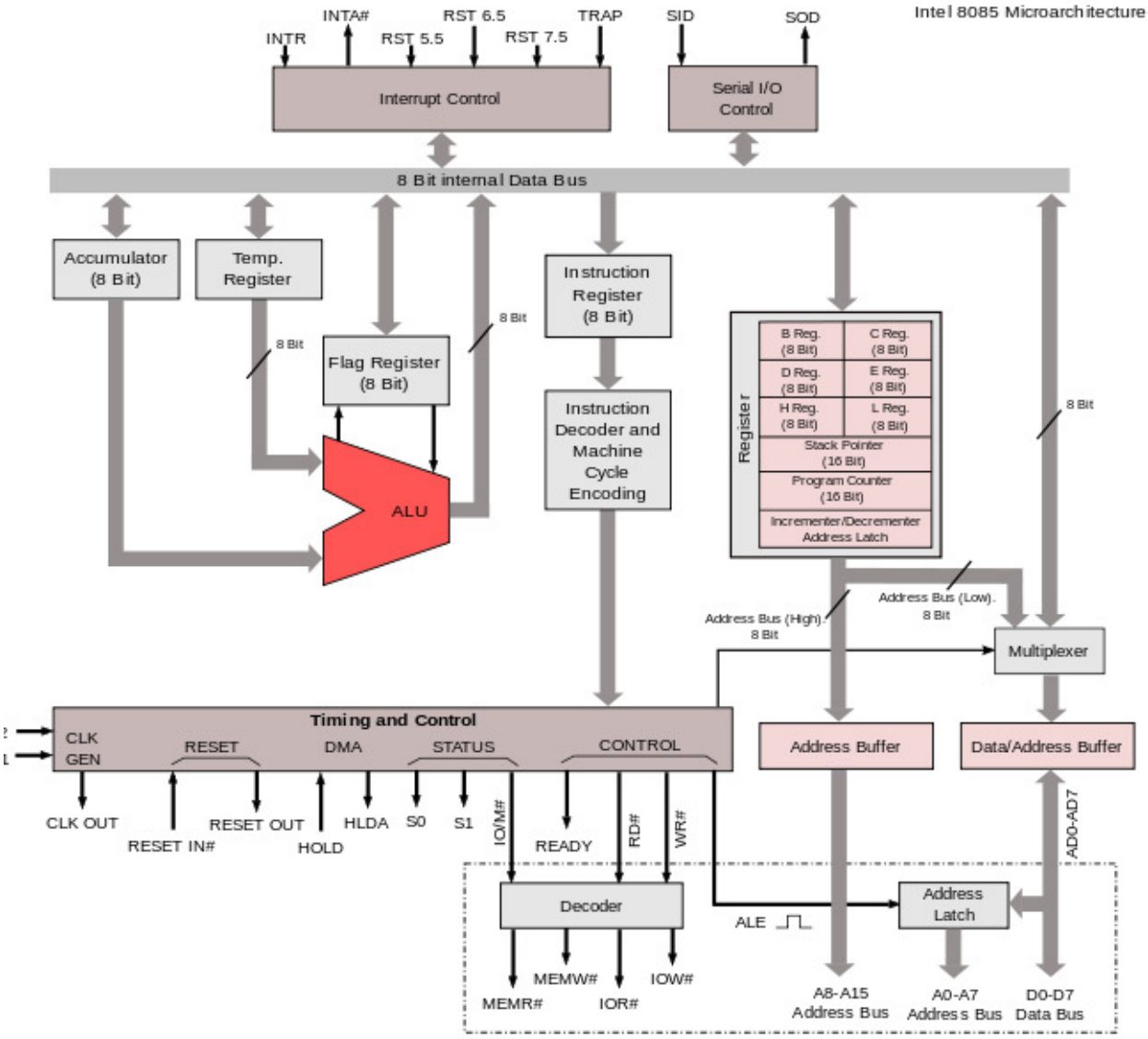
The architecture of 8085 microprocessor mainly includes the timing & control unit, Arithmetic and logic unit, decoder, instruction register, interrupt control, a register array, serial input/output control. The most important part of the microprocessor is the central processing unit.

8085 Architecture

Operations of 8085 Microprocessor

The main operation of ALU is arithmetic as well as logical which includes addition, increment, subtraction, decrement, logical operations like AND, OR, Ex-OR, complement, evaluation, left shift or right shift. Both the temporary registers as well as accumulators are utilized for holding the information throughout in the operations then the outcome will be stored within the accumulator. The different flags are arranged or rearrange based on the outcome of the operation.

Flag Registers


Intel 8085 Microarchitecture
INTR
INTA#
RST 5.5
RST 6.5
RST 7.5
TRAP
Interrupt Control
SID
SOD
Serial I/O Control
8 Bit internal Data Bus
Accumulator (8 Bit)
Temp. Register
Flag Register (8 Bit)
ALU
Instruction Register (8 Bit)
Instruction Decoder and Machine Cycle Encoding
Register
B Reg. (8 Bit)
C Reg. (8 Bit)
D Reg. (8 Bit)
E Reg. (8 Bit)
H Reg. (8 Bit)
L Reg. (8 Bit)
Stack Pointer (16 Bit)
Program Counter (16 Bit)
Incrementer/Decrementer Address Latch
8 Bit
Address Bus (High) 8 Bit
Address Bus (Low) 8 Bit
Multiplexer
Timing and Control
CLK GEN
RESET
DMA
STATUS
CONTROL
Address Buffer
Data/Address Buffer
CLK OUT
RESET IN#
RESET OUT
HOLD
HLDA
S0
S1
IO/M#
READY
RD#
WR#
AD0-AD7
Decoder
ALE
Address Latch
MEMR#
MEMW#
IOR#
IOW#
A8-A15 Address Bus
A0-A7 Address Bus
D0-D7 Data Bus

The flag registers of **microprocessor 8085** are classified into five types namely sign, zero, auxiliary carry, parity and carry. The positions of bit set aside for these types of flags. After the operation of an ALU, when the result of the most significant bit (D7) is one, then the sign flag will be arranged. When the operation of the ALU outcome is zero then the zero flags will be set. When the outcome is not zero then the zero flags will be reset.

In an arithmetic process, whenever a carry is produced with the lesser nibble, then an auxiliary type carry flag will be set. After an ALU operation, when the outcome has an even number then the parity flag will be set, or else it is reset. When an arithmetic process outcome in a carry, then carry flag will be set or else it will be reset. Between the five types of flags, the AC type flag is employed on the inside intended for BCD arithmetic as well as remaining four flags are used with the developer to make sure the conditions of the outcome of a process.

Control and Timing Unit

The control and timing unit coordinates with all the actions of the microprocessor by the clock and gives the control signals which are required for communication among the microprocessor as well as peripherals.

Decoder and Instruction Register

As an order is obtained from memory after that it is located in the instruction register, and encoded & decoded into different device cycles.

Register Array

The general purpose programmable registers are classified into several types apart from the accumulator such as B, C, D, E, H, & L. These are utilized

as 8-bit registers otherwise coupled to stock up the l6 bit of data. The permitted couples are BC, DE & HL, and the short term W & Z registers are used in the processor & it cannot be utilized with the developer.

Special Purpose Registers

These registers are classified into four types namely program counter, stack pointer, increment or decrement register, address buffer or data buffer.

Program Counter

This is the first type of special purpose register and considers that the instruction is being performed by the microprocessor. When the ALU completed performing the instruction, then the microprocessor searches for other instruction to be performed. Thus, there will be a requirement of holding the next instruction address to be performed in order to conserve time. Microprocessor increases the program when an instruction is being performed, therefore that the program counter position to the next instruction memory address is going to be performed…

Stack Pointer in 8085

The SP or stack pointer is a 16-bit register and functions similar to a stack, which is constantly increased or decreased with two throughout push and pop processes.

Increment or Decrement Register

The 8-bit register contents or else a memory position can be increased or decreased with one. The 16-bit register is useful for incrementing or decrementing program counters as well as stack pointer register content with one. This operation can be performed on any memory position or any kind of register.

Address-Buffer & Address-Data-Buffer

Address buffer stores the copied information from the memory for the execution. The memory & I/O chips are associated with these buses; then the CPU can replace the preferred data by I/O chips and the memory.

Address Bus and Data Bus

The data bus is useful in carrying the related information that is to be stock up. It is bi-directional, but address bus indicates the position as to where it must be stored & it is uni-directional, useful for transmitting the information as well as address input/output devices.

Timing & Control Unit

The timing & control unit can be used to supply the signal to the 8085 microprocessor for achieving the particular processes. The timing and control units are used to control the internal as well as external circuits. These are classified into four types namely control units like RD' ALE, READY, WR', status units like S0, S1, and IO/M', DM like HLDA, and HOLD unit, RESET units like RST-IN and RST-OUT.

8085 Microprocessor Instruction Set

The **instruction set of 8085** microprocessor is nothing but instruction codes used to achieve an exact task, and instruction sets are categorized into various types namely control, logical, branching, arithmetic, and data transfer instructions.

Addressing Modes of 8085

The addressing modes of 8085 microprocessor can be defined as the commands offered by these modes which are utilized for denoting the information in different forms without altering the content. These classified into five groups namely immediate, register, direct, indirect and implied addressing mode.

Thus, this is all about **8085 architecture**. From the above information finally, we can conclude that **8085 microprocessor features** are it is an 8-bit microprocessor, enclosed with 40-pins, uses +5V supply voltage for the operation. It consists of the 16-bit stack pointer and program counter, and 74-instruction sets, and many more. Here is a question for you, **what are the applications of 8085 microprocessor**?

Interrupts and Types of Interrupts in 8085 Microprocessor

Interrupt is signals send by an external device to the processor, to request the processor to perform a particular task or work.

Interrupts

Interrupt is signals send by an external device to the processor, to request the processor to perform a particular task or work.

- ✓ Mainly in the microprocessor based system the interrupts are used for data transfer between the peripheral and the microprocessor.
- ✓ The processor will check the interrupts always at the 2nd T-state of last machine cycle.
- ✓ If there is any interrupt it accept the interrupt and send the INTA (active low) signal to the peripheral.
- ✓ The vectored address of particular interrupt is stored in program counter.
- ✓ The processor executes an interrupt service routine (ISR) addressed in program counter.
- ✓ It returned to main program by RET instruction.

Types of Interrupts:

It supports two types of interrupts.

- ✓ Hardware
- ✓ Software

1 Software interrupts:

The software interrupts are program instructions. These instructions are inserted at desired locations in a program. The 8085 has eight software interrupts from RST 0 to RST 7. The vector address for these interrupts can be calculated as follows.

- ✓ Interrupt number * 8 = vector address
- ✓ For RST 5,5 * 8 = 40 = 28H

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- ✓ Vector address for interrupt RST 5 is 0028H

2 Hardware interrupts:

An external device initiates the hardware interrupts and placing an appropriate signal at the interrupt pin of the processor. If the interrupt is accepted then the processor executes an interrupt service routine.

The 8085 has five hardware interrupts

- ✓ TRAP
- ✓ RST 7.5

- ✓ RST 6.5
- ✓ RST 5.5
- ✓ INTR

TRAP:

- ✓ This interrupt is a non-maskable interrupt. It is unaffected by any mask or interrupt enable.
- ✓ TRAP bas the highest priority and vectored interrupt.
- ✓ TRAP interrupt is edge and level triggered. This means that the TRAP must go high and remain high until it is acknowledged.
- ✓ In sudden power failure, it executes a ISR and send the data from main memory to backup memory.
- ✓ The signal, which overrides the TRAP, is HOLD signal. (i.e., If the processor receives HOLD and TRAP at the same time then HOLD is recognized first and then TRAP is recognized).
- ✓ There are two ways to clear TRAP interrupt.

1. By resetting microprocessor (External signal)
2. By giving a high TRAP ACKNOWLEDGE (Internal signal)

RST 7.5:

- ✓ The RST 7.5 interrupt is a maskable interrupt.

✓ It has the second highest priority.

✓ It is edge sensitive. ie. Input goes to high and no need to maintain high state until it recognized.

✓ Maskable interrupt. It is disabled by,

1.DI instruction

2.System or processor reset. 3.After reorganization of interrupt.

✓ Enabled by EI instruction.

RST 6.5 and 5.5:

✓ The RST 6.5 and RST 5.5 both are level triggered. . ie. Input goes to high and stay high until it recognized.

✓ Maskable interrupt. It is disabled by,

1.DI, SIM instruction 2.System or processor reset.

3.After reorganization of interrupt.

✓ Enabled by EI instruction.

✓ The RST 6.5 has the third priority whereas RST 5.5 has the fourth priority.

INTR:

INTR is a maskable interrupt. It is disabled by,

1.DI, SIM instruction

2.System or processor reset. 3.After reorganization of interrupt

- ✓ Enabled by EI instruction.
- ✓ Non- vectored interrupt. After receiving INTA (active low) signal, it has to supply the address of ISR.
- ✓ It has lowest priority.
- ✓ It is a level sensitive interrupts. ie. Input goes to high and it is necessary to maintain high state until it recognized.

The following sequence of events occurs when INTR signal goes high.

1. The 8085 checks the status of INTR signal during execution of each instruction.

2. If INTR signal is high, then 8085 complete its current instruction and sends active low interrupt acknowledge signal, if the interrupt is enabled.

3. In response to the acknowledge signal, external logic places an instruction OPCODE on the data bus. In the case of multibyte instruction, additional interrupt acknowledge machine cycles are generated by the 8085 to transfer the additional bytes into the microprocessor.

4. On receiving the instruction, the 8085 save the address of next instruction on stack and execute received instruction.

SIM and RIM for interrupts:

- ✓ The 8085 provide additional masking facility for RST 7.5, RST 6.5 and RST 5.5 using SIM instruction.

- ✓ The status of these interrupts can be read by executing RIM instruction.

- ✓ The masking or unmasking of RST 7.5, RST 6.5 and RST 5.5 interrupts can be performed by moving an 8-bit data to accumulator and then executing SIM instruction.

- ✓ The status of pending interrupts can be read from accumulator after executing RIM instruction.

- ✓ When RIM instruction is executed an 8-bit data is loaded in accumulator, which can be interpreted as shown in fig.