# Lesson Plan

**Name of the Faculty member:** **Sh. Vipul Pant**

**Discipline:** **Computer Engg.**

**Semester:** **3rd**

**Subject:** **Digital Electronics**

**Lesson Plan duration:** **w.e.f. 22nd July-16th Nov, 2019 ( tentative )**

| Week | Theory | | Practical | |
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| | **Lecture day** | **Topic Covered (Including Assessment and Sessionals)** | **Practical day** | **Topic Covered ( Including Viva-Voce)** |
| 1st | 1. | Introduction to Digital Electronics, Analog signals, Digital Signals | 1. | Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates (Gr-A) |
| | 2. | Distinction b/w Analog & Digital Signals | 2. | Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates (Gr-B) |
| | 3. | Applications and advantages of Digital Signals | | |
| 2nd | 4. | Number System: Binary, Octal, Decimal & Hexadecimal, Conversion exercises | 3. | Same Practical Repeated (Gr-A) |
| | 5. | Conversion exercises on fractional numbers | 4. | Same Practical Repeated (Gr-B) |
| | 6. | Binary addition & subtraction. Subtraction using 1's & 2's Complement method | | |
| 3rd | 7. | Revision of 1st & 2nd Unit | 5. | Realization of Logic Functions with the help of NAND & NOR gates (Gr-A) |
| | 8. | Codes and Parity: Concept of code, Weighted & Non weighted code, eg. BCD | 6. | Realization of Logic Functions with the help of NAND & NOR gates (Gr-B) |
| | 9. | Excess-3 code, Gray code, conversion from binary to Gray code and vice versa | | |
| 4th | 10. | Concept of Parity- Single and Double parity | 7. | To design a half adder using a NAND & XOR gates and verification of its operations (Gr-A) |
| | 11. | Error Detection using Single parity | 8. | To design a half adder using a NAND & XOR gates and verification of its operations (Gr-B) |
| | 12. | Logic Gates and Families: Introduction to Logic Gates, Negative and Positive logic | | |
| 5th | 13. | Definitions, Symbols & Truth tables of NOT, AND, OR, NAND & NOR gates | 9. | Construction of a full adder using a NAND & XOR gates and verification of its operations (Gr-A) |
| | 14. | Definitions, Symbols & Truth tables of EX-OR & EX-NOR gates | 10. | Construction of a full adder using a NAND & XOR gates and verification of its operations (Gr-B) |
| | 15. | NAND & NOR gates as Universal gates, Introduction to TTL & CMOS logic families | | |
| 6th | 16. | Revision of 3rd & 4th Unit | 11. | Repetition of Practical's for Those who came Late (Gr-A) |
| | 17. | Logic Simplification: Boolean algebra-Postulates, Laws and Theorems of Boolean algebra | 12. | Repetition of Practical's for Those who came Late (Gr-B) |
| | 18. | De Morgan's Theorem with truth table, implementation of Boolean equation with gates | | |

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| 7th | 19. | Karnaugh map( K-map) upto 4-variables in developing simple combinational logic circuits | 13. | Lab Performance & Viva-Voce (Gr-A) |
| | 20. | Exercise on K-map | 14. | Lab Performance & Viva-Voce (Gr-B) |
| | 21. | **1st sessional Test** | | |
| 8th | 22. | Arithmetic Circuits: Half Adder & Full Adder Circuit- Design and Implementation, 4- bit Parallel binary adder design | 15. | Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-A) |
| | 23. | Decoder: Introduction & 4-bit decoder circuit for seven segment display | 16. | Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-B) |
| | 24. | Multiplexer: Introduction, basic functions and block diagrams with different IC's | | |
| 9th | 25. | De multiplexer : Introduction, basic functions and block diagrams with different IC's | 17. | Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-A) |
| | 26. | Encoder: Introduction, basic functions and block diagrams with different IC's | 18. | Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-B) |
| | 27. | Revision of 5th, 6th, and 7th Unit | | |
| 10th | 28. | Latches and Flip Flops: Concept of a Latch, types, working & applications | 19. | Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-A) |
| | 29. | Flip Flop- Introduction, Defn, types RS, D,JK, T AND Master Slave Flip Flop | 20. | Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-B) |
| | 30. | Explanation of their working with truth table and wave form diagram | | |
| 11th | 31. | Applications of Flip Flops, Difference b/w Latch & Flip Flop | 21. | Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-A) |
| | 32. | Counters: Definition, Types- Synchronous and Asynchronous Counters, Their Difference | 22. | Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-B) |
| | 33. | Binary counters: Explanation with truth Table and diagram, 2-bit, 3-bit counters | | |
| 12th | 34. | Mod-N or Divide by N counters: Examples with truth Table and diagram | 23. | To design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-A) |
| | 35. | Decade Counter( both Synchronous & Asynchronous): Design | 24. | o design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-B) |
| | 36. | Up/Down Asynchronous and Synchronous Counters | | |
| 13th | 37. | Ring Counter and Johnson Counter | 25. | To design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-A) |
| | 38. | **2nd Sessional Test** | 26. | o design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-B) |
| | 39. | Shift Register: Introduction & basic Concept of shifting Left and Right, Types | | |
| 14th | 40. | SISO, SIPO: Explanation with block diagram & Truth Table | 27. | Lab Performance & Viva-Voce (Gr-A) |
| | 41. | PISO & PIPO: Explanation with block diagram & Truth Table | 28. | Lab Performance & Viva-Voce (Gr-B) |
| | 42. | Universal Shift Register | | |
| 15th | 43. | A/D & D/A Converters: Introduction & working Principle | 29. | To design a 4-bit Ring Counter and verify its operations(Gr-A) |
| | 44. | Different Techniques of A/D conversion & Study of Stair Step Ramp A/D converter | 30. | To design a 4-bit Ring Counter and verify its operations(Gr-B) |
| | 45. | Study of Dual Slope and Successive Approximation A/D converter | | |

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| 16th | 46. | Detail study of Binary Weighted D/A converter | 31. | To design a 4-bit Ring Counter and verify its operations(Gr-A) |
| | 47. | Detail Study of R/2R Ladder D/A converter, Applications of A/D & D/A converter | 32. | To design a 4-bit Ring Counter and verify its operations(Gr-B) |
| | 48. | Semiconductor memories : Memory Organization, Classification of Semiconductor memories | | |
| 17th | 49. | RAM: DDRAM, SRAM, ROM: PROM, EPROM,EEPROM | 33. | Use of Asynchronous Counter IC'S (7490 OR 7493) (Gr-A) |
| | 50. | Introduction to 74181 IC | 34. | Use of Asynchronous Counter IC'S (7490 OR 7493) (Gr-B) |
| | 51. | **3rd Sessional Test** | | |