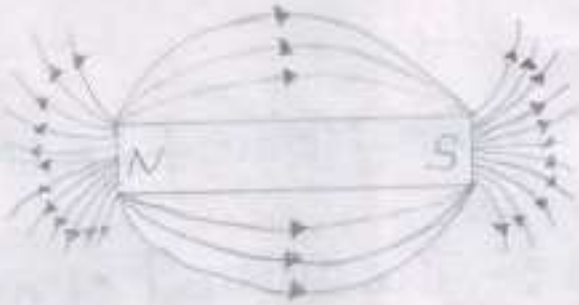
Electro Magnetic Induction

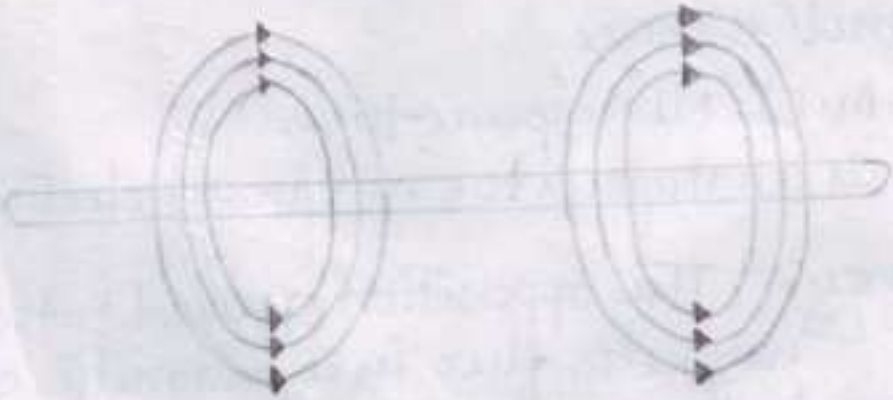
Magnetic field :— The area around a magnetic pole or a magnet. within which its influence is observed is called its magnetic field



Magnetic effect of electric current

When an electric current flows through a conductor magnetic field is set up all along the length of the conductor.

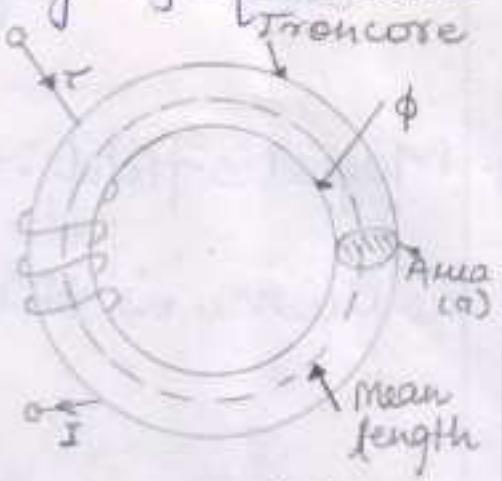
The direction of lines of force is given by right hand rule.



Magnetic circuit

The closed path followed by magnetic flux is called magnetic circuit. A magnetic circuit usually

Consists of magnetic materials having high permeability. e.g. iron, soft steel etc.



$$H = \frac{NI}{\text{mean length}}$$

Concept of flux, Magneto-Motive force (MMF) / Reluctance

1) Magnetic flux (ϕ) :- The amount of magnetic lines of force set up in a magnetic circuit is called magnetic flux. It unit is weber (wb) It is analogous to electric current (I) in an electric circuit.

2) Magnetomotive force (MMF) :- The magnetic pressure which set up or tends to set up magnetic flux in a magnetic circuit is called magnetomotive force.

(m.m.f) = NI ampere-turns

It is analogous to e.m.f in an electric circuit

3) Reluctance (S) :- The opposition offered to the flow of magnetic flux in a magnetic circuit is called its reluctance.

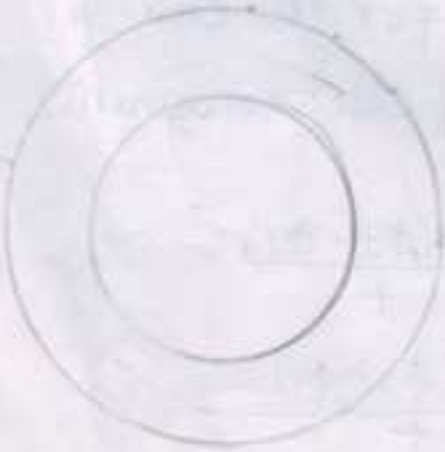
It depend upon length (l), area of cross-sectional (a) and permeability (μ) of the material that makes the magnetic field.

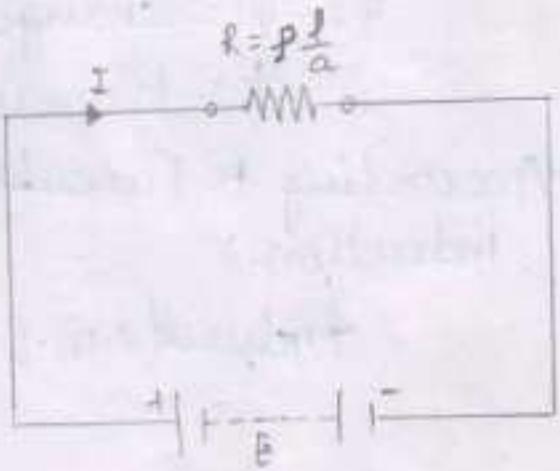
$$\text{Reluctance}(S) = \frac{l}{a\mu_0\mu_r} \qquad | \mu = \mu_0\mu_r$$

4) Permeability :- The ability of a material to conduct magnetic flux through it is called permeability of that material.

Analogy between Magnetic and Electric circuits

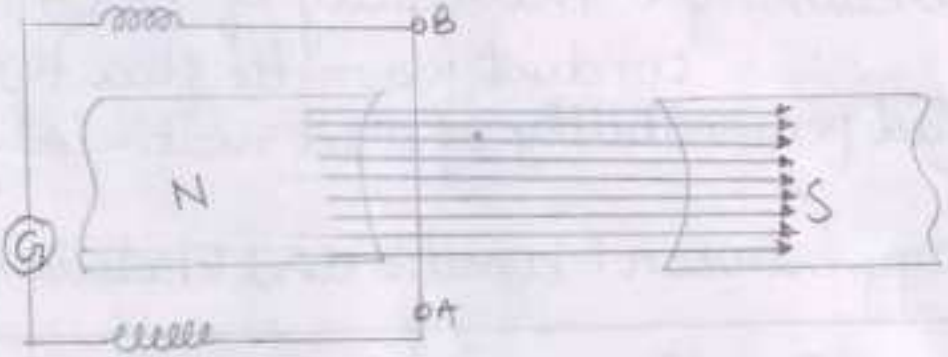
Magnetic circuit	Electric circuit
1) The close path for magnetic flux is called magnetic circuit	1) The closed path for electric circuit is called electric circuit
2) flux = m.mf / Reluctance	2) Current = emf / resistance
3) flux, ϕ in weber	3) Current, I in ampere.
4) m.mf in AT	4) e.m.f in V.
5) permeability, μ.	5) conductivity, σ $\mho/p$
6) Reluctance, $S = \frac{l}{a\mu} = \frac{l}{a\mu_0\mu_r}$ AT/wb	6) Resistance, $R = \rho\frac{l}{a}$ Ω





electric circuit

Electromagnetic Induction :— When flux linking with a Conductor changes, an e.m.f. is included in it



Faraday's law of electro-Magnetic Induction

Faraday's First law :— When the flux linking with the coil or circuit changes an emf is introduced in it.

Faraday's second law :— The magnitude of emf induced is directly proportional to the rate of changes of flux linkage and to be number of turn of the coil.

Rate of change of flux linkage $= \frac{N(\phi_2 - \phi_1)}{t}$

where, N = No. of turns of the coil

$\phi_2 - \phi_1$ = change of flux in weber (wb)

t = time in second for the change

According to Faraday's law of electromagnetic Induction.

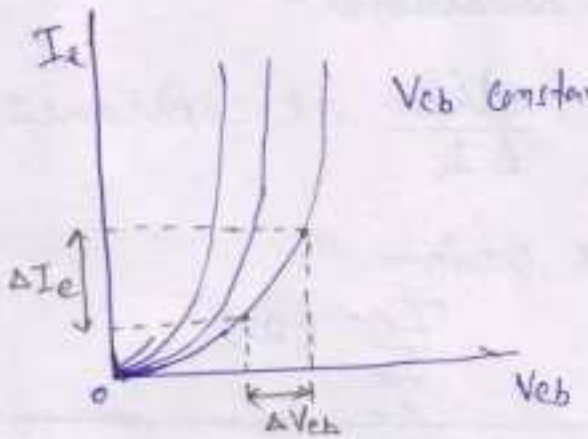
Induced e.m.f., $e \propto \frac{N(\phi_2 - \phi_1)}{t}$

$$e = \frac{N(\phi_2 - \phi_1)}{t}$$

#CB configuration of n-P-n configuration-

- In CB configuration of transistor, when we take n-p-n transistor there is common base between the emitter and collector.
- The base is forward biased with the emitter and Reversed with the collector.
- Emitter current (I_e) flows from the n-type and collector current (I_c) flows from the n-type.
- In CB configuration current flow from P-type to N-type.

Input characteristics of CB configuration of n-p-n transistor-



This characteristic shows the variation of emitter current (I_e) w.r.t V_{EB} when V_{CB} is kept constant

V_{CB} is the voltage between collector and base

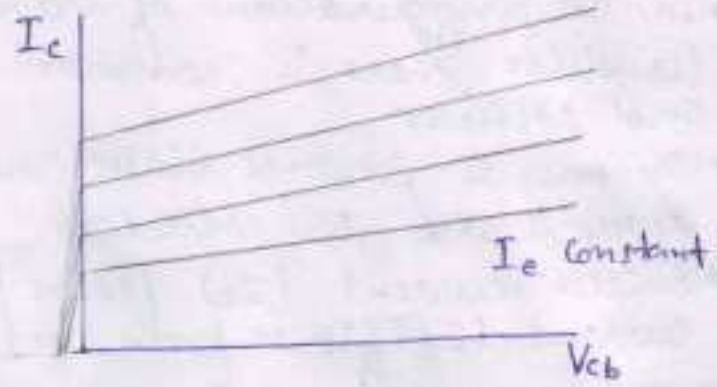
Input resistance-

$$R_{in} = \frac{\Delta V_{EB}}{\Delta I_E}$$ where V_{CB} is constant

V_{EB} = Voltage b/w emitter and base

It is also known as Dynamic Input resistance

Output characteristics of CB configuration-



This characteristics indicates the variation of output current (I_c) wrt variation of V_{CB} (Voltage b/w collector and base) when Input current (I_E) is kept constant.

Output resistance-

$$R_O = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

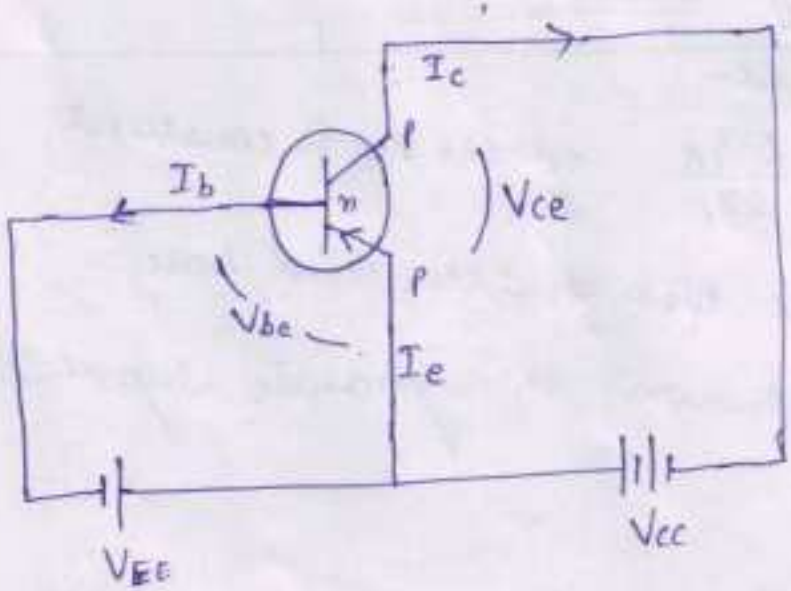
Current Gain-

$$\frac{I_c}{I_e} \ (\alpha)$$

Voltage Gain-

$$\frac{V_{cb}}{V_{cb}}$$

Characteristics of transistor in CE configuration.



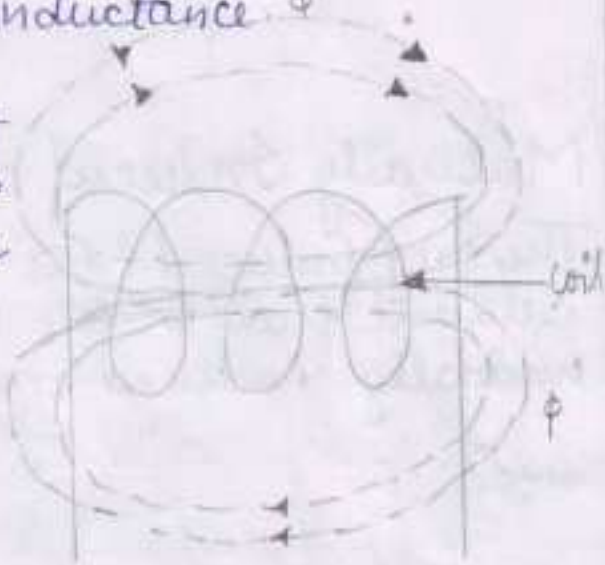
In differential form, $e = N\frac{d\phi}{dt}$ volts.

Usually minus sign given to right hand side hand indicate that emf induced opposes the cause that produce it, also known as Lenz's Rule

$$e = -N\frac{d\phi}{dt} \text{ volts.}$$

Principal of Self-Inductance

The property of a circuit, by which an emf is induced in the circuit whenever the current flowing through it changes, is termed as self inductance.



Consider a coil N-turns carrying a current of I amp. Let the flux linking with the coil be (ϕ) weber

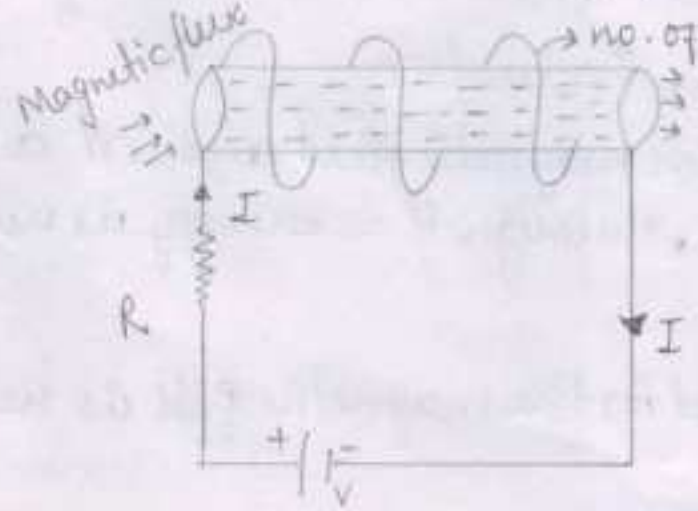
Then, flux linkages = NI

The emf so induced is called self induced emf.

Self induced emf.

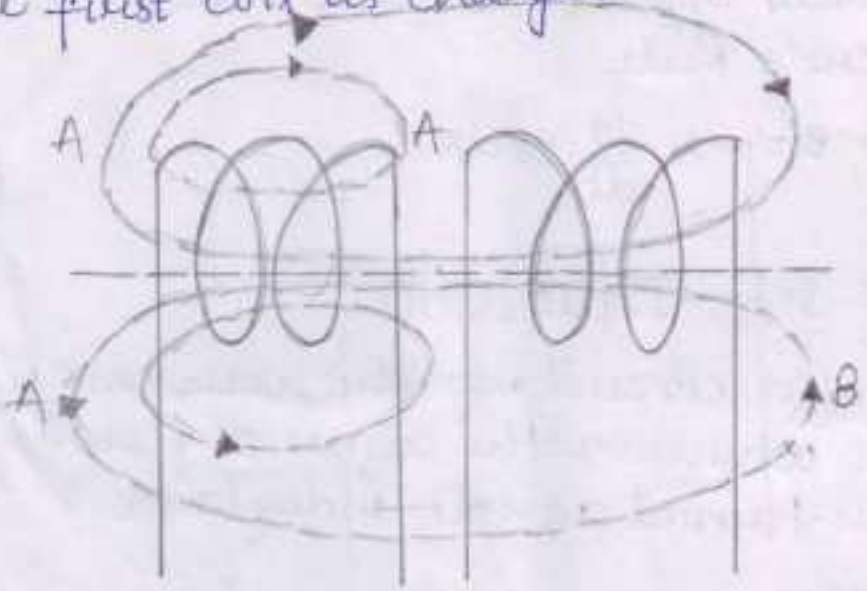
The emf induced in a coil due to the change of own magnetic flux is called self induced emf

Self induced emf = $N\frac{d\phi}{dt}$ [According to faraday's IInd law



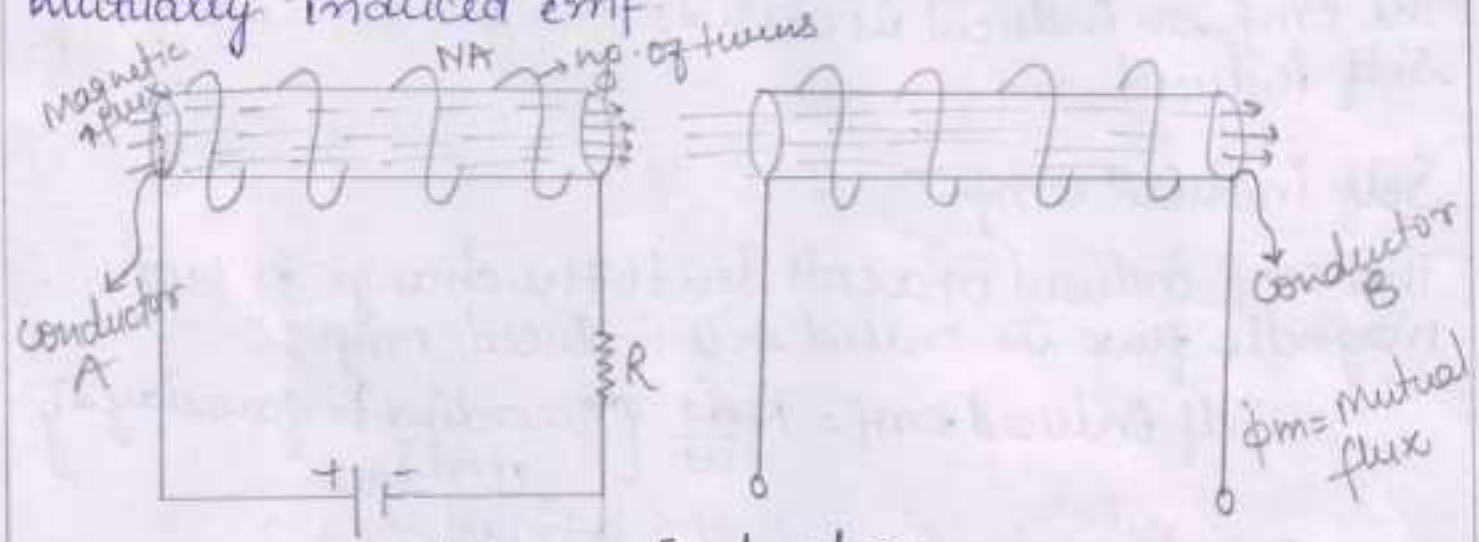
Principal of Mutual Induction.

The ability of one coil or circuit to induce an emf in a nearby coil by induction when the current flowing in the first coil is changed.



Mutually Induced emf.

The emf induced in a coil due to the changing current flux in the neighbouring coil is called mutually induced emf



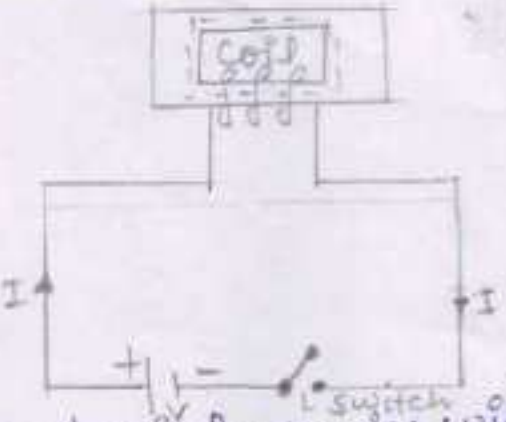
Energy Stored in an inductor

1) In order to establish magnetic field around a coil, energy is required, through this energy is not needed to maintain it.

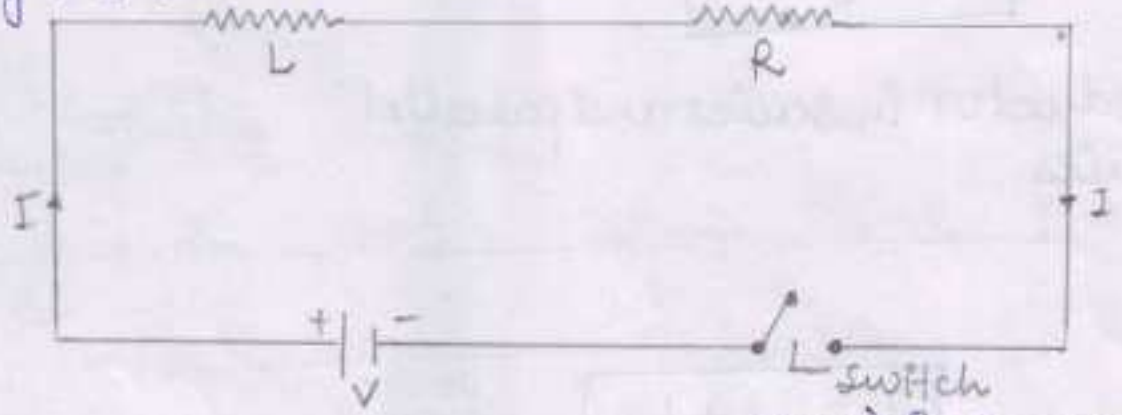
2) This energy is stored in the magnetic field is not used

3) When current ↓ = mag. flux ↓ Caused the stored energy to be returned to the circuit

→ In fig.1 consider coil inductor is connected to the DC source.



→ In fig.2 Inductor is in series with Resistance (R)



4) The energy supplied to the source spent in two ways

(i) Spent to meet I^2R losses

(ii) Remaining part is spent to create magnetic flux around the coil and is stored in magnetic field.

$$e = L\frac{di}{dt} \quad \text{——— (I)}$$

$$\text{Power} = ei \quad \text{——— (II)}$$

Putting the value of e in eq^n (II)

$$P = \left[L\frac{di}{dt}\right] i$$

$$P = L\left[i\frac{di}{dt}\right]$$

Now,

$$\text{work} = \int P\,dt \quad \text{——(iii)}$$

Putting the value of P in eqn (iii).

$$W = \int Li\frac{di}{dt}\,dt$$

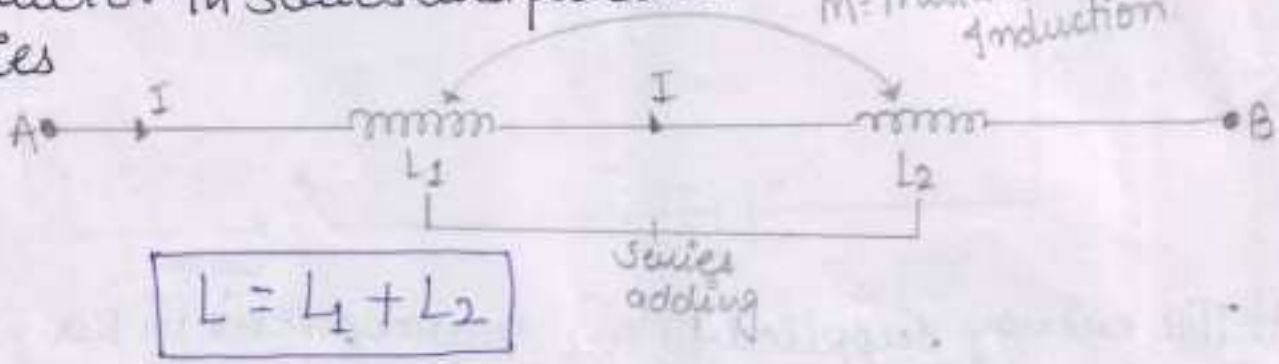
$$W = \int Li\,di$$

$$W = L\frac{i^2}{2}$$

$$\boxed{W = \frac{1}{2}Li^2}$$

Inductor in series and parallel

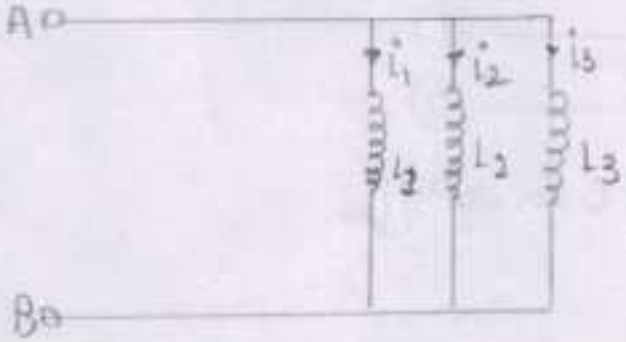
Series



$$\boxed{L = L_1 + L_2}$$

Series = current same
= voltage change.

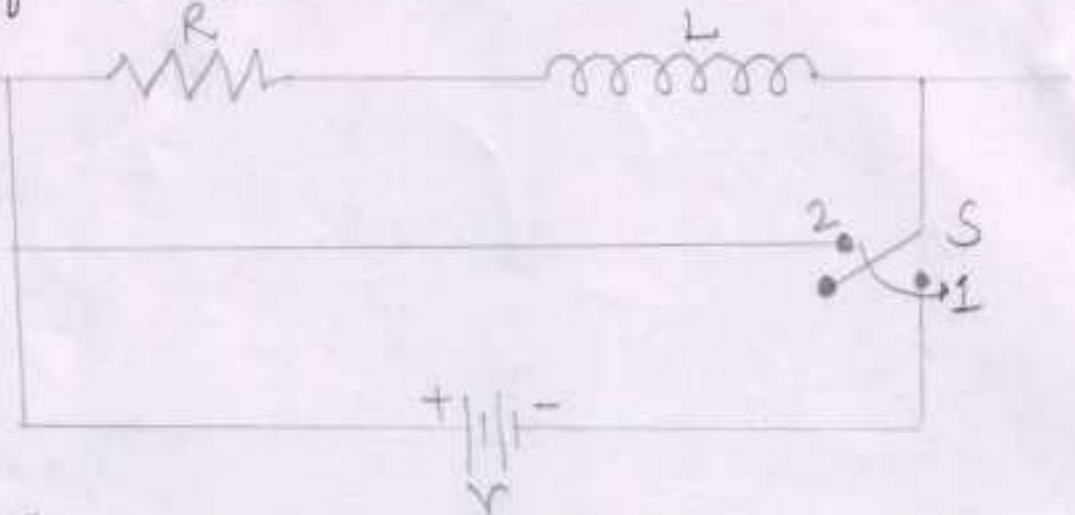
Parallel



$$\boxed{\frac{1}{L} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}}$$

Parallel = current change
= voltage same

Rise of current in an inductor



Let initially the switch 'S' is at position 1. The voltage equation for the circuit shown for the circuit shown in ∫

$$V = iR + L\frac{di}{dt} \quad \text{——— (I)}$$

$$V - iR = L\frac{di}{dt} \quad \text{——— (II)}$$

$$\frac{di}{(V-iR)} = \frac{dt}{L} \quad \text{——— (III)}$$

Multplying equation (III) both side with $(-R)$ we get,

$$\frac{(-R)\,di}{(V-iR)} = \frac{(-R)}{L}\,dt \quad \text{——— (IV)}$$

Now, integration both side, we get

$$\int \frac{(-R)\,di}{(V-iR)} = \int \frac{(-R)}{L}\,dt$$

INTRODUCTION TO BIPOLAR-TRANSISTOR

Transistor (Bipolar) - A device having two junctions and three terminals. It is sandwich of n-type semi-conductor between two p-type semi-conductor or vice-versa.

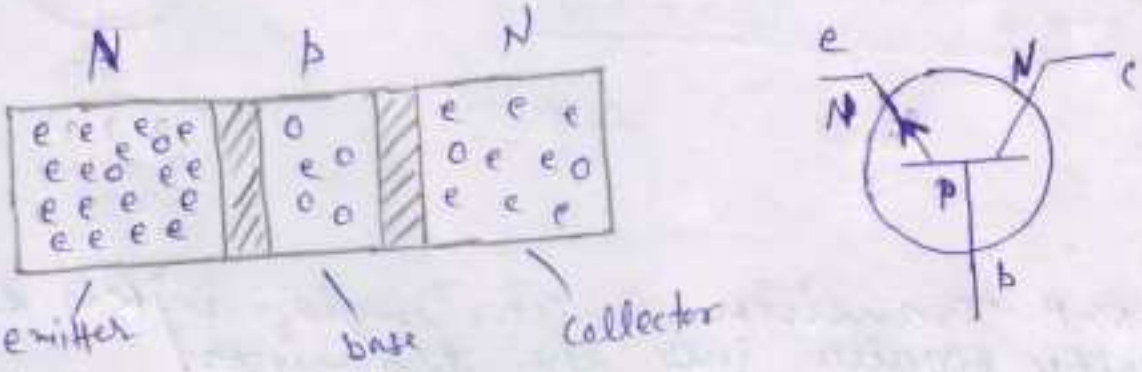
These two junctions give rise to three regions called emitter, base and collector. ①

Types of transistor:-

1) N-P-N Transistor-

P-type semiconductor is sandwich between two n-type semi-conductor.

Diagram and symbol of NPN



In N-PN transistor, Emitter region injects the majority carriers of electrons into the transistor.

The emitter is heavily doped with electrons and has medium width.

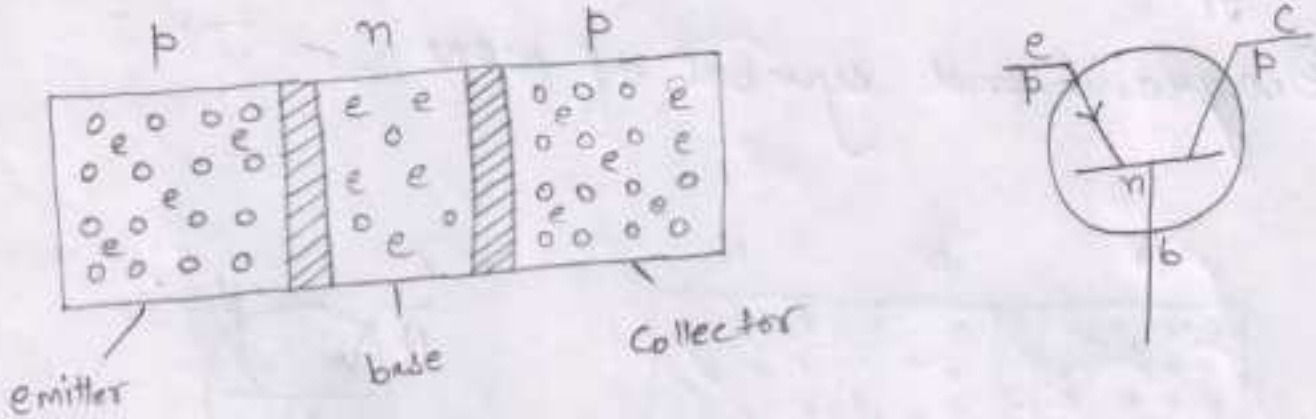
Base- Base portion is the middle portion of transistor which contain holes as the majority carriers and supports the emitter and collector

Collector It is mediumly doped with electrons as majority carriers. It collects all the majority carriers.

2. P-N-P Transistor -

N-type semiconductor is sandwich between two P-type semiconductors.

Diagram and symbol of P-N-P



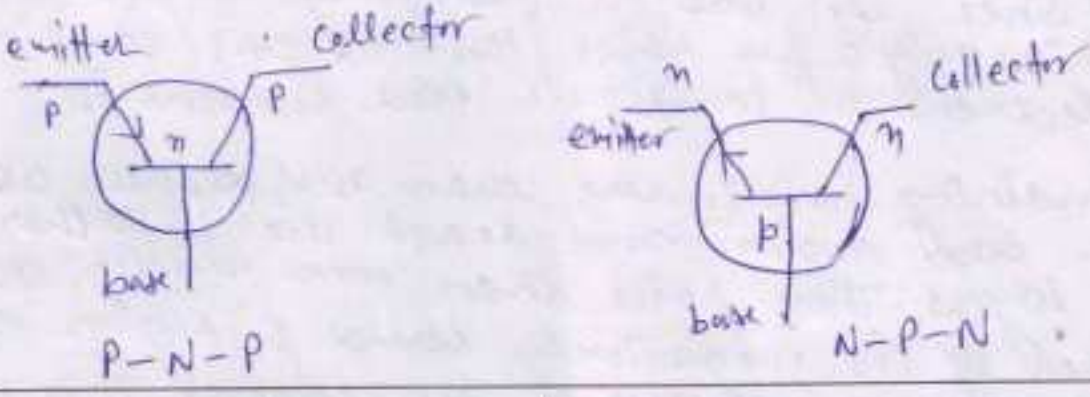
In P-N-P Transistor, Emitter region injects the majority carrier into the transistor.

The emitter region is heavily doped with holes and has medium width

Base- The P-N-P junction, base is doped with the electrons as the majority carriers.

Collector - It is mediumly doped with holes as the majority carriers.

Symbols of PN-P & N-P-N transistor

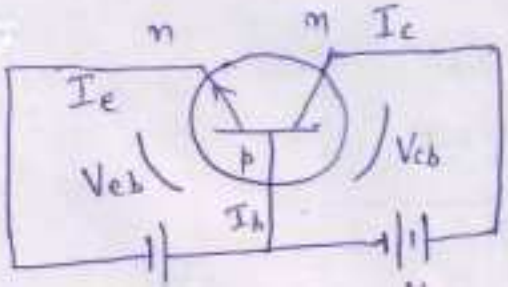


Mechanism of current flow -

An npn transistor circuit is shown in fig. here. The forward bias voltage V_{EB} is quite small, whereas reverse bias voltage V_{CB} is considerably high.

As the emitter base junction is forward biased, a large no. of electrons (majority carriers) in the emitter (n-type region) are pushed towards the base. This constitutes the emitter current I_E. When these electrons (more than 95%) diffused across the thin base region and reach the collector space charge layer. These electrons are attracted or collected by the collector. This constitutes collector current I_C. The emitter currents is the sum of collector current and base current.

$$\text{i.e.} \quad I_E = I_C + I_B$$



A pnp transistor circuit shown here. The forward bias voltag V_{EB} is considerably high.

As the emitter-base junction is foward biased, a large no of holes (majority carrier) in the emitter (p-type semi-conductor) are pushed together the base. This constitutes the emitter current I_E. When these holes enter the n-type material (base), they tends to combine with electrons. Since the base is slightly doped and very thin, only a few holes (less than 5%) combine with electrons to constitute base current I_B.

The remaining holes (more than 95%) diffuse across the thin base region and reach the co-e. space charge layers. These holes than come under the influenced of the negatively biased p-region and are attracted or collected by the collector. This constitutes collector current I_C. Almost the entire emitter current flows in to the collector circuits. The emitter current is the sum of collector current and base current. i.e.,

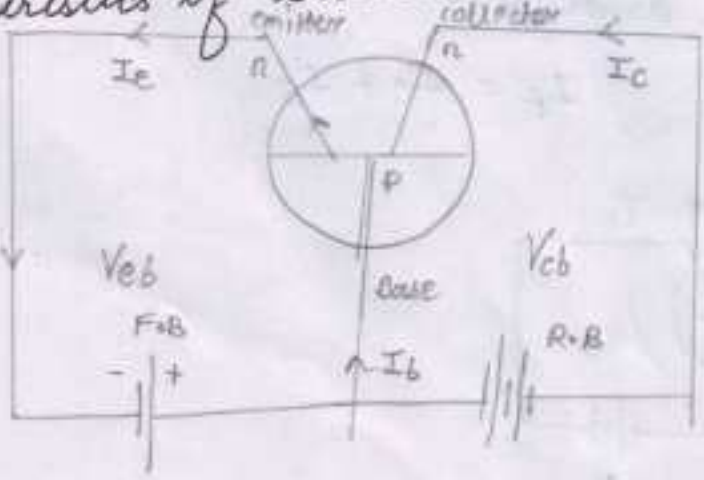
$$I_E = I_C + I_B$$

Current relation in trasistor –

Emitter Current = base current + Collector Current

$$I_E = I_B + I_C$$

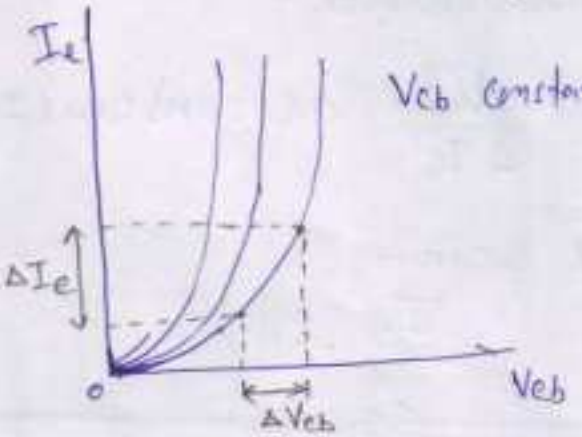
Characteristics of transistor in CB configuration –



#CB configuration of n-P-n configuration-

- In CB configuration of transistor, when we take n-p-n transistor there is common base between the emitter and collector.
- The base is forward biased with the emitter and Reversed with the collector.
- Emitter current (I_e) flows from the n-type and collect current (I_c) flows from the n-type.
- In CB configuration current flow from p-type to N-type

Input characteristics of CB configuration of n-p-n transistor-



This characteristic shows the variation of emitter current (I_e) w.r.t V_{EB} when V_{CB} is kept constant

V_{CB} is the voltage between collector and base

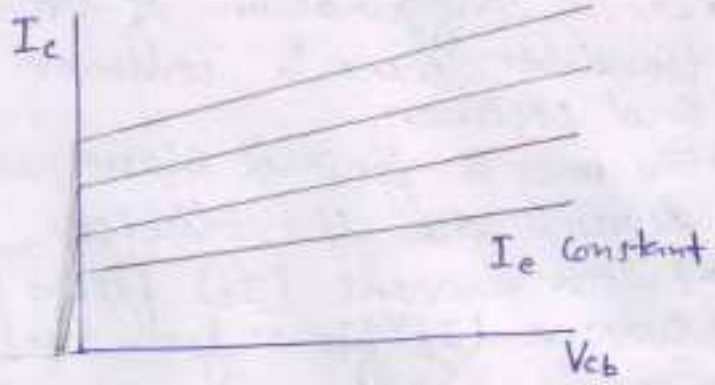
Input resistance-

$$R_{in} = \frac{\Delta V_{EB}}{\Delta I_E}$$ where V_{CB} is constant

V_{EB} = Voltage b/w emitter and base

It is also known as Dynamic Input resistance

Output characteristics of CB configuration-



This characteristics indicates the variation of output current (I_c) w.r.t variation of V_{CB} (Voltage b/w collector and base) when Input current (I_E) is kept constant.

Output resistance-

$$R_O = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

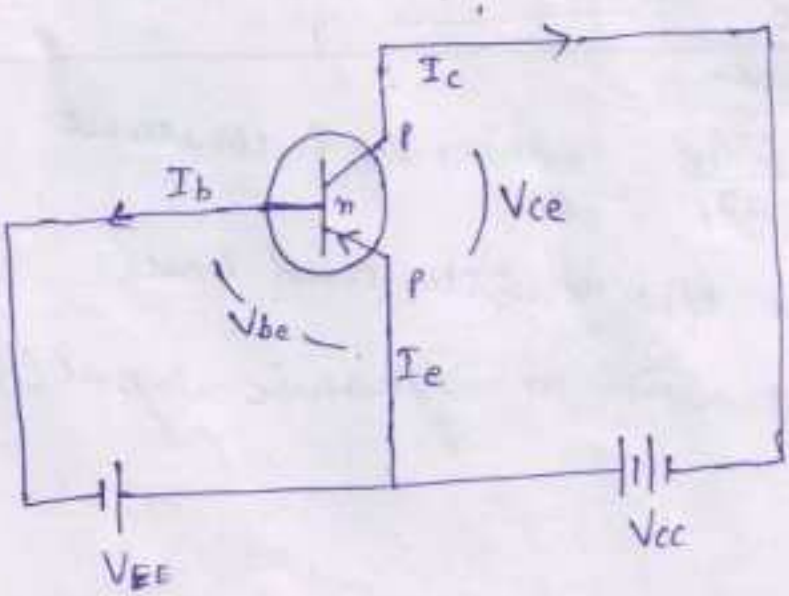
Current Gain-

$$\frac{I_c}{I_e} \ (\alpha)$$

Voltage Gain-

$$\frac{V_{cb}}{V_{cb}}$$

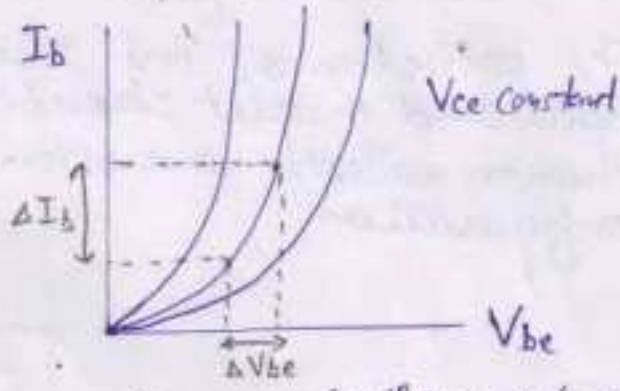
Characteristics of transistor in CE configuration.



- The CE configuration of transistor when we take P-N-P transistor, there is common emitter between the base and collector.
- The base is forward biased with the emitter.
- And the collector is Reversed biased with the emitter.
- Base current is (I_B) flows from the n-type and collector current (I_C) flows from the p-type.

In CE configuration the current flows from the p-type to n-type.

Input characteristics of CE configuration -



Input characteristics of shows the variations of I_B w.r.t. variation V_{BE} and V_{CE} is kept constant.

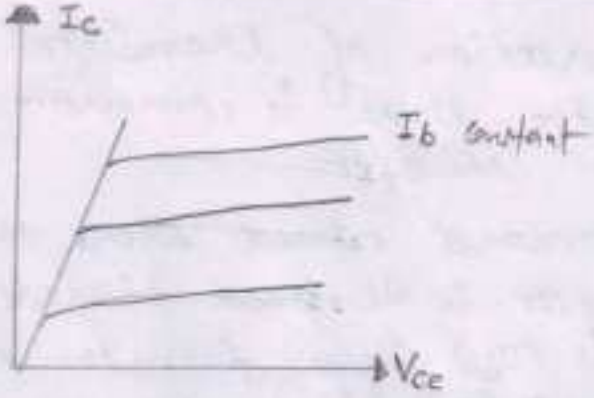
V_{CE} is voltage between collector and emitter.

Dynamic Input resistance of CE configuration of P-N-P Transistor -

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{when } V_{CE} \text{ is constant}$$

Dynamic Output characteristics -

This characteristics shows the variation of output current I_C with change in the output voltage (V_{CE}) when, the input current (I_B) is kept constant.



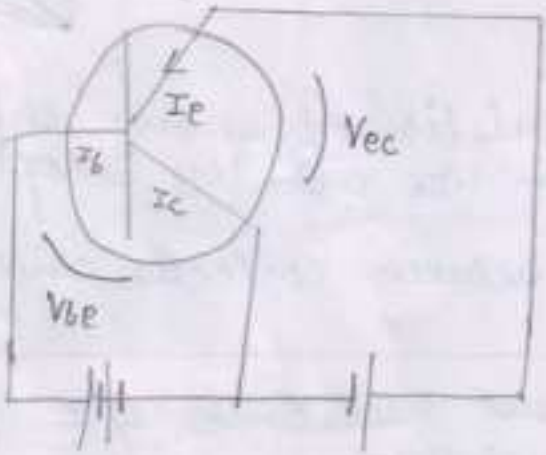
Output resistance –

$$R_{out} = \frac{\Delta V_{CE}}{\Delta I_C}$$ when I_B is constant

---

Characteristics of transistor in CC configuration–

The collector of the transistor is common to both input and output circuits and hence the name common collector connection or common collector configuration.



Current gain- $\frac{I_c}{I_e}$ (α)

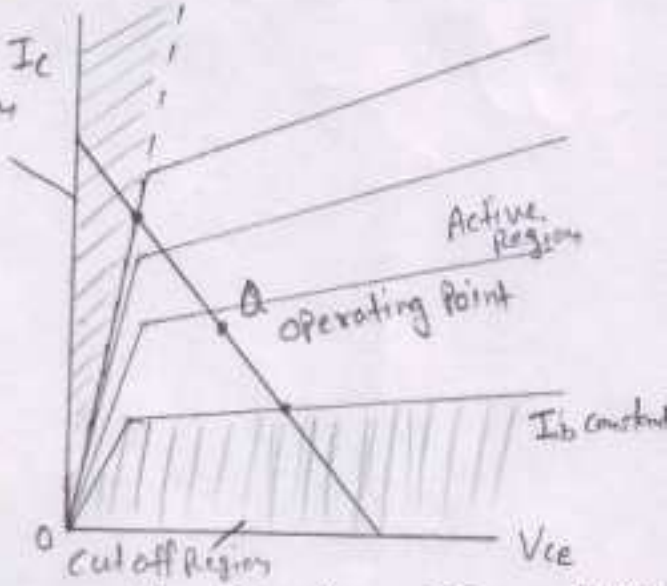
Comparison between transistor in CB, CE & CC configuration

Sr no	Particulars	CB	CE	CC
1.	Input impedance	Low (upto 50Ω)	Low (upto 1K)	Very high (750
2.	Output impedance	Very high (480K)	high (40K)	Low (50μ
3.	Current gain	less than unity	high (upto 400)	high upto 400
4.	Voltage gain	small (150)	high (about 450)	Less than 1
5.	Leakage current	Between 2μA & 5μA	Between 20μA and 5μA	Between 20μA and 4-50μA
6.	Application	For high frequency amplification	For audio frequency amplification	For impedance matching

DC load line –

The line drawn on output characteristics showing relation of between output voltage and current in the absence of input signal. For e.g. DC load line

For common emitter configuration can be shown as given below.



Ac from output ckt

$V_{cc} = V_{ce} + I_c R_c \rightarrow (1)$

if $V_{ce} = 0$

$(1) \Rightarrow V_{cc} = I_c R_c \Rightarrow$

$\Rightarrow I_c = \frac{V_{cc}}{R_c} \rightarrow (2)$

if $I_c = 0$

$(1) \Rightarrow V_{cc} = V_{ce} \rightarrow (3)$

Plotting Graph using equation (2) & (3) we get DC Load Line.

Concept of leakage current in Bipolar Transistor

The leakage current in any transistor is due to the movement of minority carriers.

This leakage current flows into the collector lead and out of the base lead. This small collector current is called collector leakage current when

- It is represented by → I_{CBO}
- It signifies the current between collector and base with emitter terminal open

Q what is saturation region in Transistor?
when both emitter & base as well as collector-base junctions are forward biased

Q what is cut-off region in Transistor?
when both emitter & base as well as collector-base junction are reverse biased.

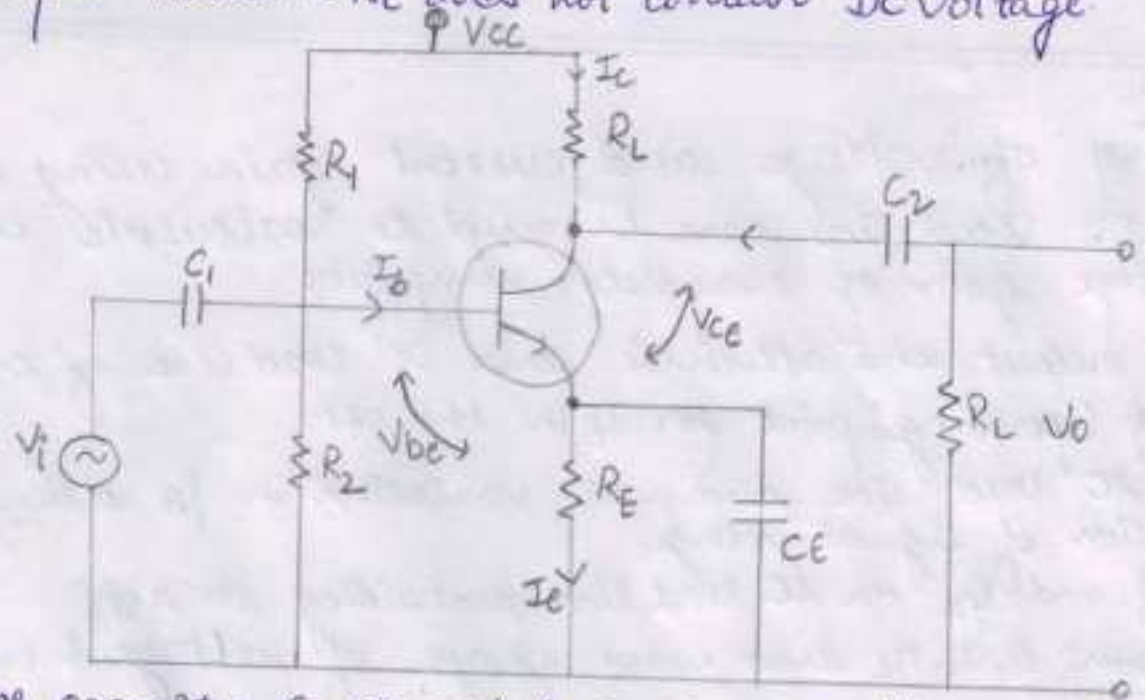
Single Stage Amplifier

Amplifier: A device used to amplify work signal.

CE Amplifier: A transistor in CE configuration can be used as amplifier after suitable biasing.

Fig. show CE configuration of transistor biased in active region, using Potential divider circuit.

The capacitor C_1 & C_2 are connected to isolate input and output signal from D.C supply. These capacitors are known as coupling capacitors. They block the flow of DC current so that the output across R_L does not contain DC voltage



The capacitor C_E connected across emitter resistance R_E works as bye pass capacitor. It provide low resistance path for A.C to flow through it. Otherwise the voltage across R_E will provide negative feedback and which reduce the gain of amplifier.

The resistance X_{CE} offered by capacitor C_E to lower frequency AC signal must be small.

$$X_{CE} \ll R_E/10$$

The resistance R_L is used to take output across it.

Voltage gain is defined as the ratio of output voltage to input voltage.

$$A_V = \frac{V_0}{V_i} \quad (A.C.)$$

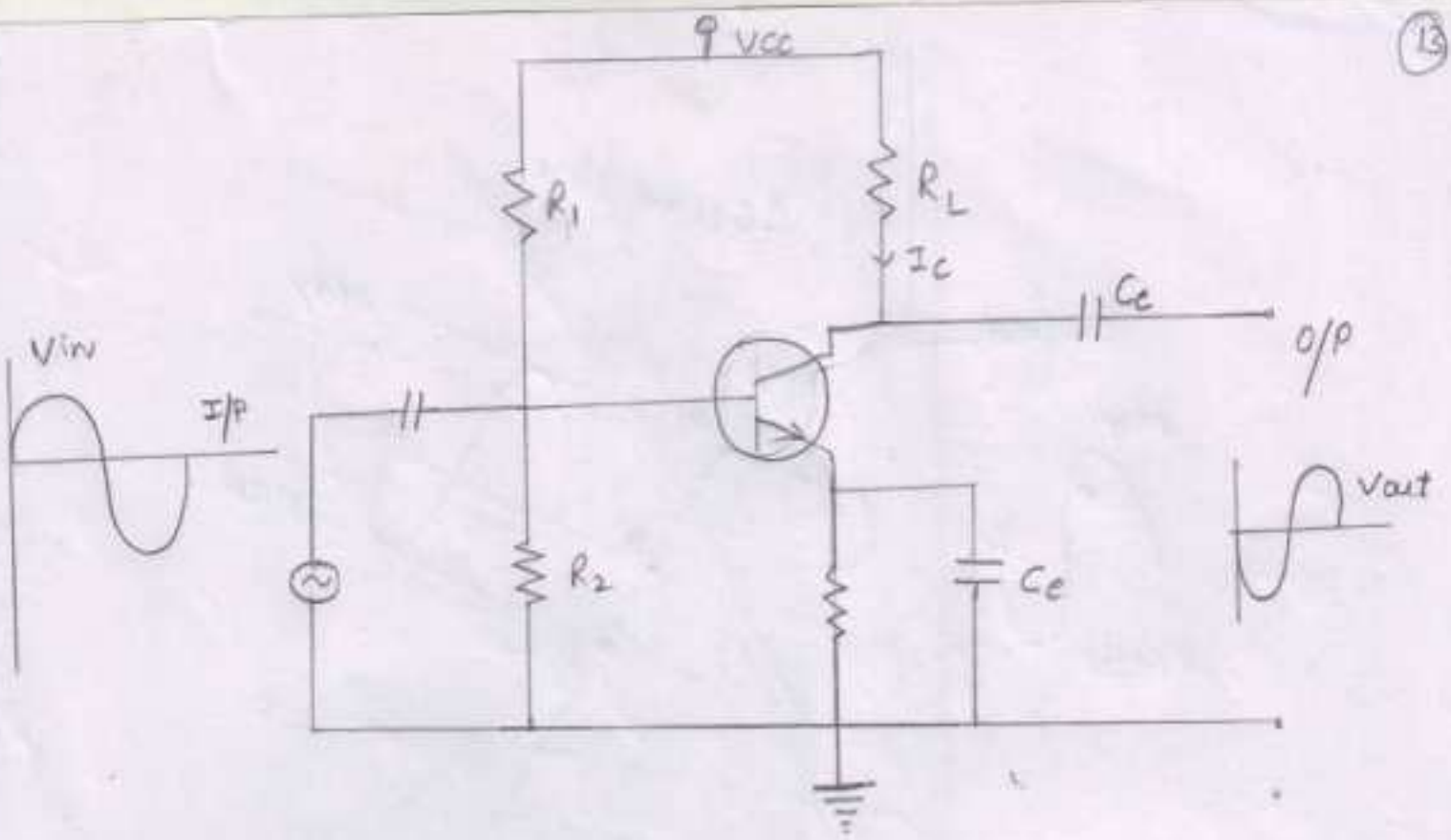
Mostly, a single stage amplifier does not give required amplification, so multistage amplifier and then required

Calculation of voltage and current Gain using Loadline

AC and DC load line can be used to calculate current and voltage gain of transistor amplifier.

i) Draw output characteristic and DC load line of transistor
ii) locate Q (operating) point for I_B in the ckt.
iii) Draw AC load line and peak variation in i_B due to application of signal voltage.
iv) locate Q_1 and Q_2 on AC load line pertaining to Δi_B.
v) From point Q, Q_1, Q_2 draw wave shape of voltage & current.

This shows variation of I_b, V_{ce}, I_c from minimum to maximum value.



An AC signal is applied at I/P terminal (base emitter jn). The output is taken across load Rc or across CE jn (Vce) using KVL for O/P terminal

$$V_{CC} = V_{ce} + I_c R_c$$
$$V_{Ce} = V_{CC} - I_c R_c \longrightarrow (1)$$

With increase in +ve half cycle of AC signal, the Bias potential for emitter junction is increased, which increase base current and hence I_c, Thus output V_{ce} decreases (eqn 1). We can say that when input voltage Vin increases in +ve half cycle, the output voltage (Vout) decrease. Hence, there is a phase difference of 180° in I/P and O/P voltage. This is phase reversal.

H-Parameters (Hybrid parameters)

A transistor can be considered as two part network

V_1, I_1 is input and V_2, I_2 is output voltage & current respectively

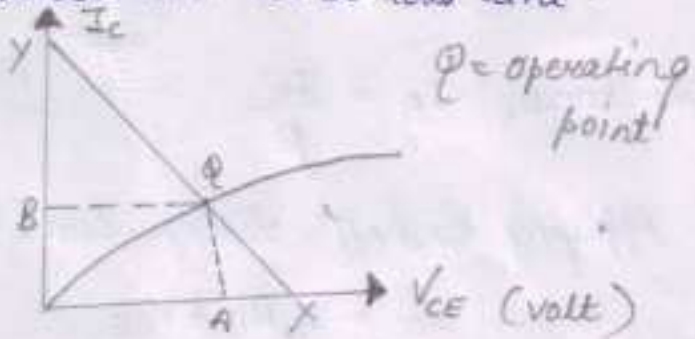
Chapter - II

Transistor Biasing Circuit

Operating Point

It is defined as a point determined by the value of I_c and V_{ce} in the absence of a.c signal.

In the absence of input signal, operating point is at Q where the output characteristic curve intersects with the DC load line.



Here, $I_c = OB$ (in mA)

$V_{CE} = OA$ (in Volt)

[I_c ⇒ collector current
V_{CE} ⇒ voltage between collector and emitter]

Need for Stablization

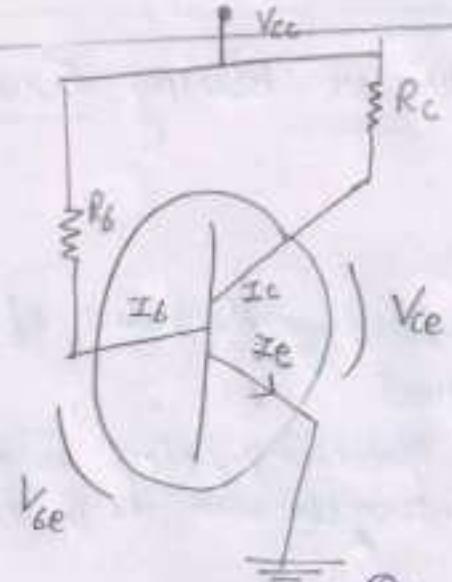
The operating point may shift into cut-off or saturation region when input signal is applied it may also shift due to change in other parameter like temperature also in that case the amplifier give improper amplification and destroyed signals. so, we need to stablized the operating point in active region for proper working of transistor

Types of transistor Baising Circuit

There are four types of transistor biasing

1) Fixed Bias (base resistor biasing)

The base resistor biasing for an npn transistor. Here a high resistance R_B is connected between the positive end of the supply and the base.



As we know, $I_B = \frac{I_C}{\beta}$ ①

Applying kirchoff's voltage law (KVL) to the base emitter loop

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since the value of V_{BE} is quite small as compared to V_{CC}, it is generally neglected

$$I_B = \frac{V_{CC}}{R_B}$$

V_{CC} is a fixed known value and I_B is fixed by the operating conditions, therefore, this biasing method is sometimes called fixed biasing method.

Applying kirchoff's voltage law (KVL) is collector emitter loop

$$V_{CC} = I_C R_C + V_{CE}$$

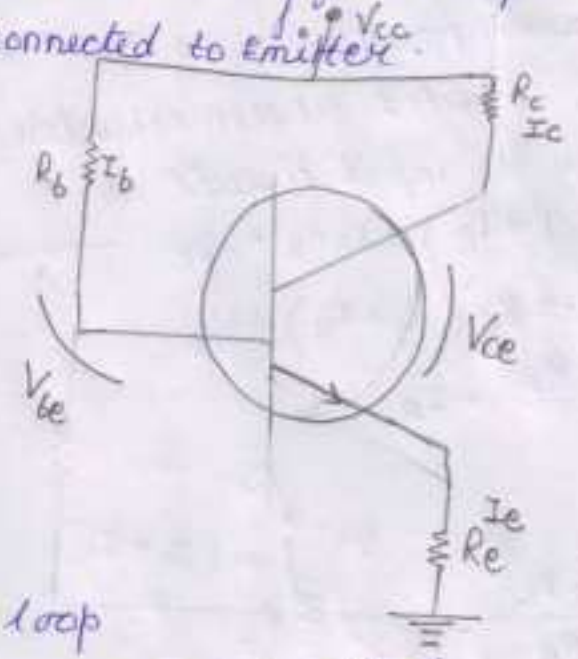
$$V_{CE} = V_{CC} - I_C R_C$$

Advantages

* In this biasing method, calculations are simple.
* Simple in construction.
* There is no loading of the source.

Emmeter field back baising

The emmeter resistor biasing for an npn transistor. here, a resistance is connected to emitter.



From, the fut loop

$$V_{cc} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{cc} = I_B R_B + V_{BE} + (\beta+1) I_B R_E \quad [\text{since } I_E = (\beta+1) I_B]$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E}$$

Neglecting V_{BE} since it is very small

$$I_B = \frac{V_{cc}}{R_B + \beta R_E}$$

collector current

$$I_C = \beta I_B = \frac{\beta V_{cc}}{R_B + \beta R_E}$$

$$= \frac{V_{cc}}{R_E + \frac{R_B}{\beta}}$$

writing the loop equation for the output circuit

$$V_{cc} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{cc} - (R_C + R_E) I_C \quad \text{——} (3)$$

Advantages

i) It provides for better stabilisation

Collector to Base Biasing (Feedback Resistor Biasing)

The feedback Resistor biasing is also known as collector to base Biasing. this biasing arrangement for an npn transistor. Here, a high resistance R_2 is connected between collector and base.

The loop equation for the input circuit is

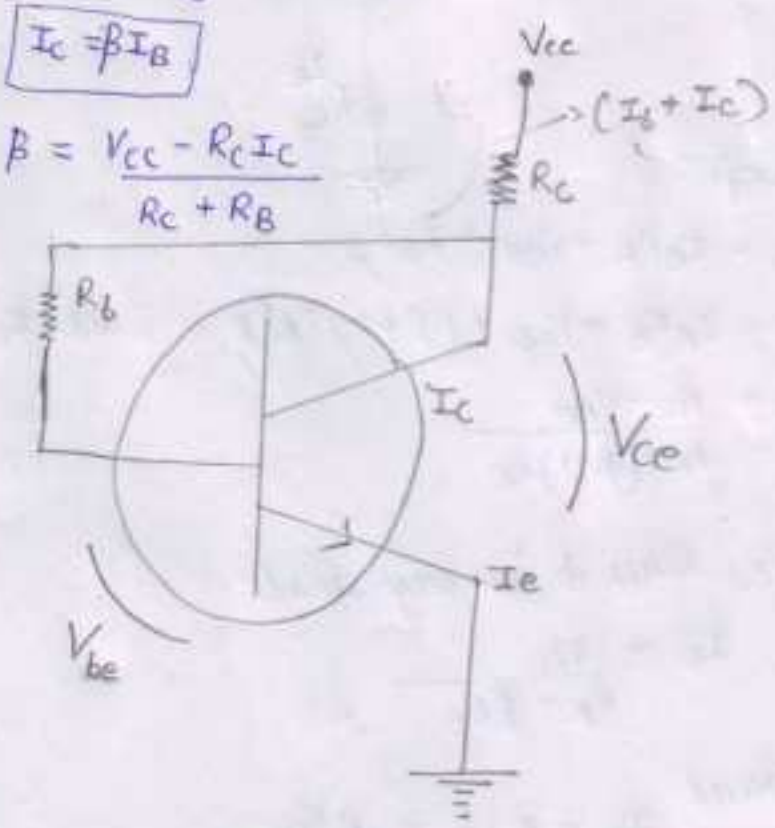
$$V_{CC} = R_C(I_C + I_B) + I_B R_B + V_{BE} \quad \text{——— (1)}$$

$$V_{CC} = I_C R_C + I_B(R_C + R_B) + V_{BE}$$

$$\frac{V_{CC} - R_C I_C - V_{BE}}{R_C + R_B} = I_B$$

$$\boxed{I_C = \beta I_B}$$

$$\beta = \frac{V_{CC} - R_C I_C}{R_C + R_B}$$



writing writing loop equation for the output circuit, we get

$$V_{CC} = V_{CE} + (I_C + I_B) R_C$$

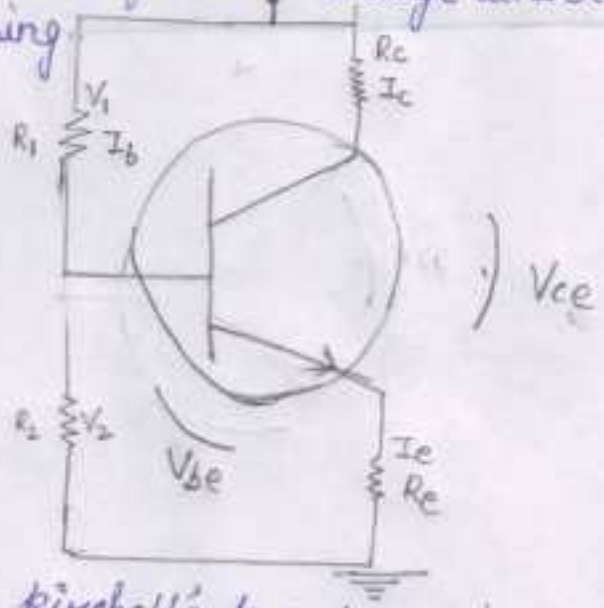
$$V_{CE} = V_{CC} - I_C R_C \quad (\text{neglected } R_C I_B)$$

Advantages

* It is biasing arrangement as only one resistor R_B is required.
* The biasing circuit provides some stablisation of the operating point.

Potential Divider Baising (voltage)

The voltage divider biasing for an npn transistor. In this biasing circuit, two resistors R_1 and R_2 are connected across the supply voltage V_{cc} and provide the necessary biasing whereas a resistor is connected in the emmiter circuit R_E provides stability since the resistors R_1 and R_2 from the voltage divider hince the name voltage divider biasing



Applying Kirchoff's law to the input circuit, we get

$$V_{cc} = I_1 R_1 + I_1 R_2$$

$$I_1 = \frac{V_{cc}}{R_1 + R_2}$$

Voltage across Resistor R_2,

$$V_2 = I_1 R_2 = \left[\frac{V_{cc}}{R_1 + R_2}\right] R_2 \quad \text{---- (1)}$$

writing loop equation in the base emitter circuit

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E \qquad (\text{since, } V_E = I_E R_E)$$

$$I_E = \frac{V_2 - V_{BE}}{R_E} \quad \text{---- (2)}$$

$$I_C \cong I_E$$

$$I_C = \frac{V_2 - V_{BE}}{R_E}$$

In all pratical circuits $V_2 \gg V_{BE}$ therefore V_{BE} in

comparison to V_2

Applying kirchoff's law

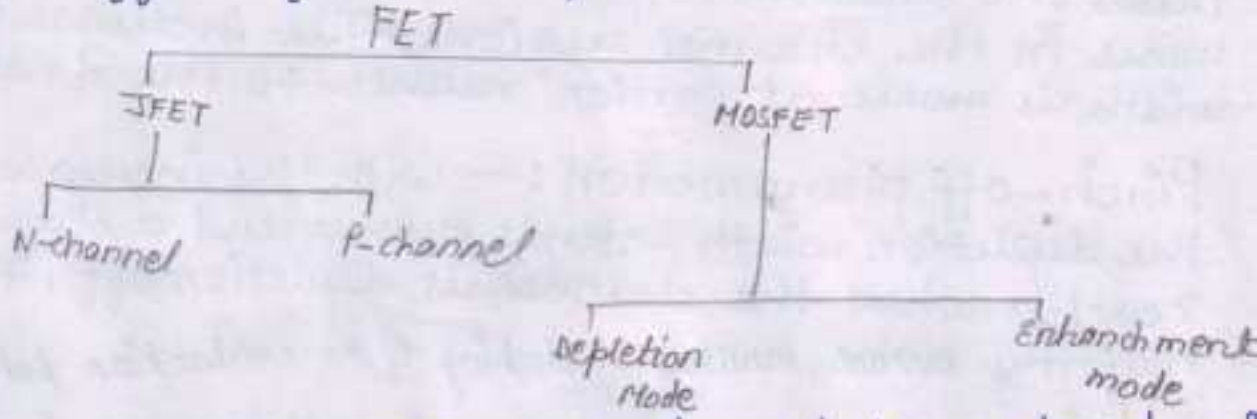
$$V_{cc} = I_c R_c + V_{CE} + I_E R_E$$

$$V_{cc} = I_c R_c + V_{CE} + I_c R_E$$

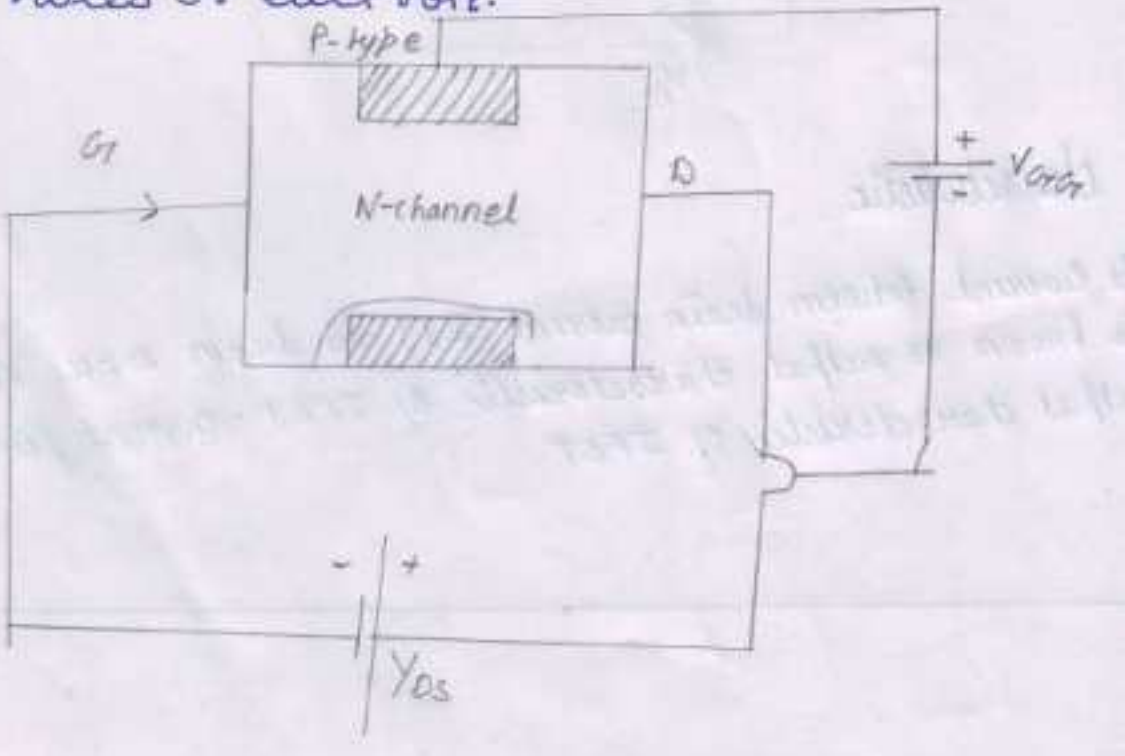
$$V_{CE} = V_{cc} - I_c (R_c + R_E) \quad \text{—— (4)}$$

field Effect transistor

Junction field Effect transistor (JFET) :- Junction field effect transistor is a three terminal semi-conductor dence in which current condition is by the flow of one type of carriers and is controlled by the effect of electric field.

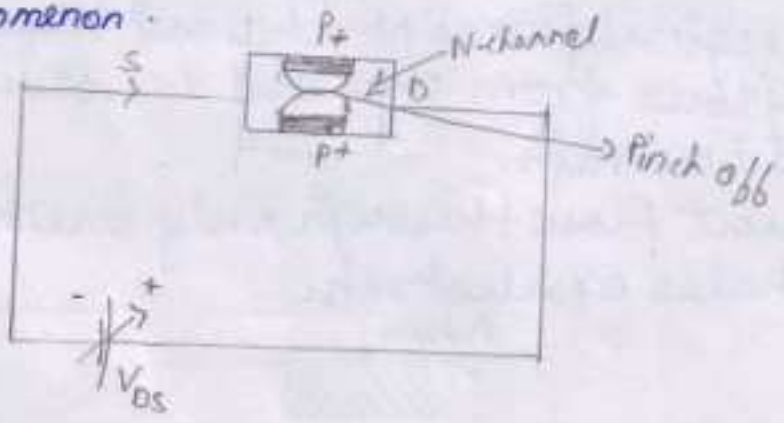


Construction:- In FET N-type bar between two heavily doped P-regions forms N-channel through which current flows from one end. i.e. source of the other end i.e. drain.
The current flow through only one type of charge carriers holes or electron.



Working :— The gate to source junction is reverse baised since the gate is doped more heavily than the channel, the depletion ~~layer~~ width extends more in the channel. Initially, let us assume that $V_{GS} = 0$, when V_{DS} is increased, the drain current goes on increasing. But with the increased V_{DS}, the reverse bias on the gate source junctions also increase Thus, the depletion ~~layer~~ width increase and is more in the channel regions. The increase in width is more at portion nearer to the drain.

Pinch-off phenomenon :— with the increased V_{DS}, the depletion width extends more and a stage reaches when the channel is depletion off, the majority carriers, resulting in blocking of the conduction path and the drain current becomes constant. such a phenomenon is called pinch-off phenomenon.



Characteristic

The current between drain current (I_d) and drain source voltage (V_{DS}). is known as output characteristic of JFET. Current for determining output characteristic of JFET.

*.

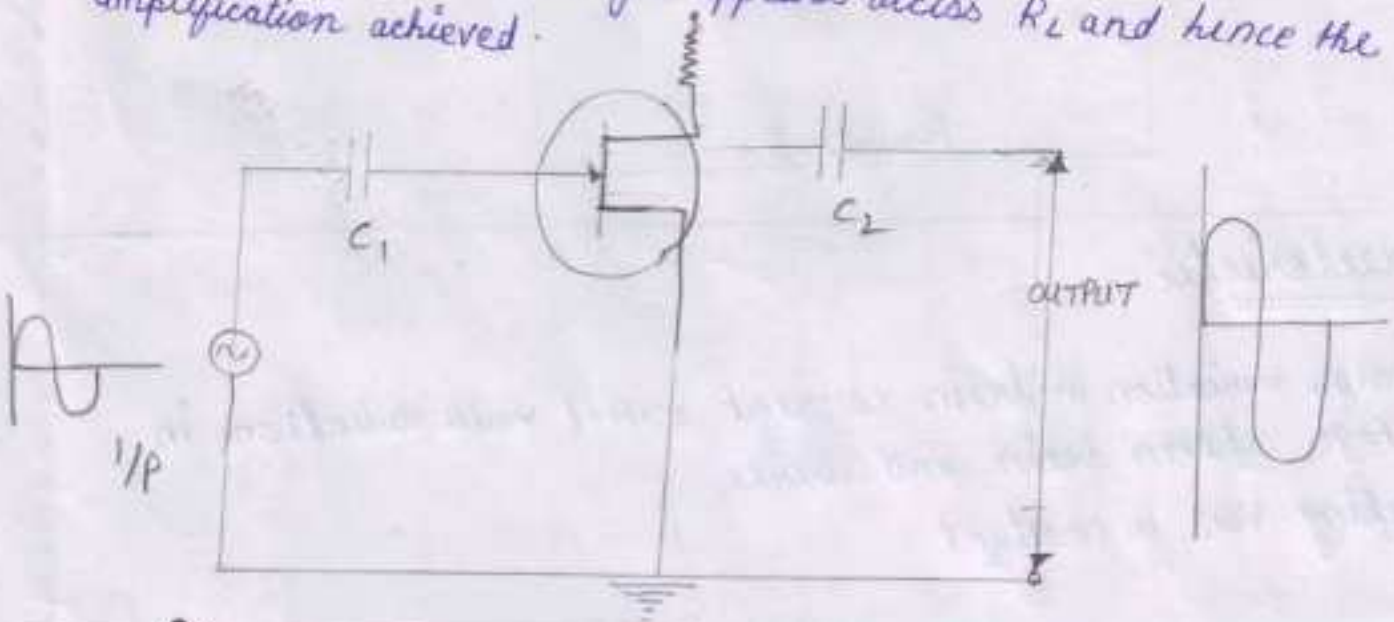
FET as an amplifier

* The gate source circuit is reverse biased due to which the deplution layer is formed and the channel width is reduced, resulting in flow of constant drain current.

* When a weak-signal is applied accross the gate and source, the reverse bias decrease during +ve half cycle of input signal. This increases channel width accordingly drain current increases.

* During the negative half cycle, the channel width decreases, and drain current also decreases. Thus a small change in input signal result in large change in the drain current through the load resistance R_L.

* Thus, a large output voltage appears accuss R_L and hence the amplification achieved.



Reversal in common / emitter / transistor amplifier

MOSFET

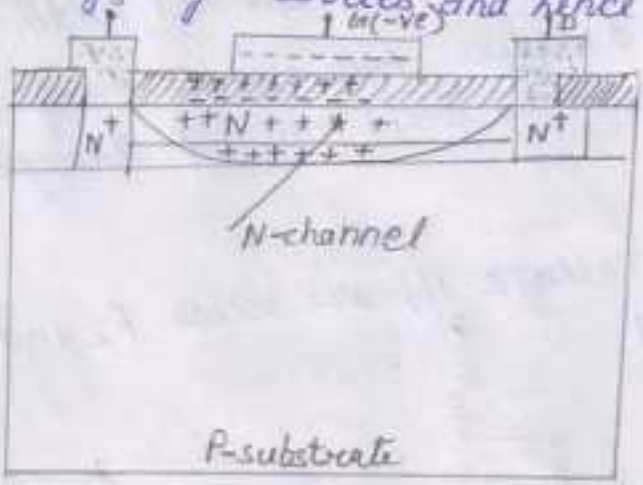
Metal oxide semiconductor field effect transistor. It consist of lightly doped P-substate in which two heavily doped N+region are diffused. A thin layer of insulating silicon-dioxide is then grown over the surface and holes are cut into this layer for making contacts with drain and source.

Working

The n-channel is formed by diffusion between source and drain, the result is depletion-type MOSFET.

When -ve voltage is applied at the gate +ve charge induced in the n-channel through the insulating layer of SiO_2

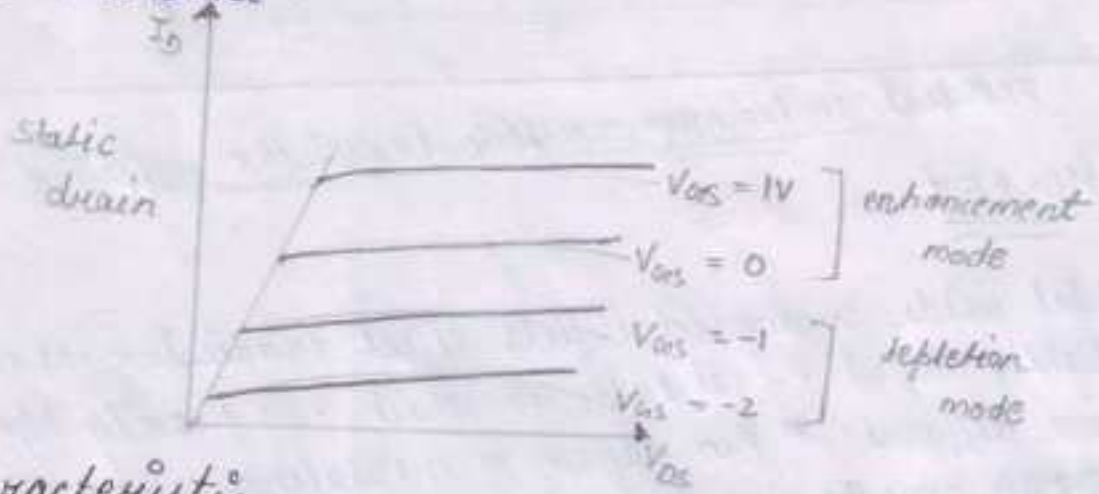
Thus, the drain current reduces as the voltage V_{GS} is made more negative. the new distribution of charges in the channel results in depletion of majority carries and hence named as depletion MOSFET.



Characteristic

It shows variation in drain current w.r.t variations in voltage between drain and source.

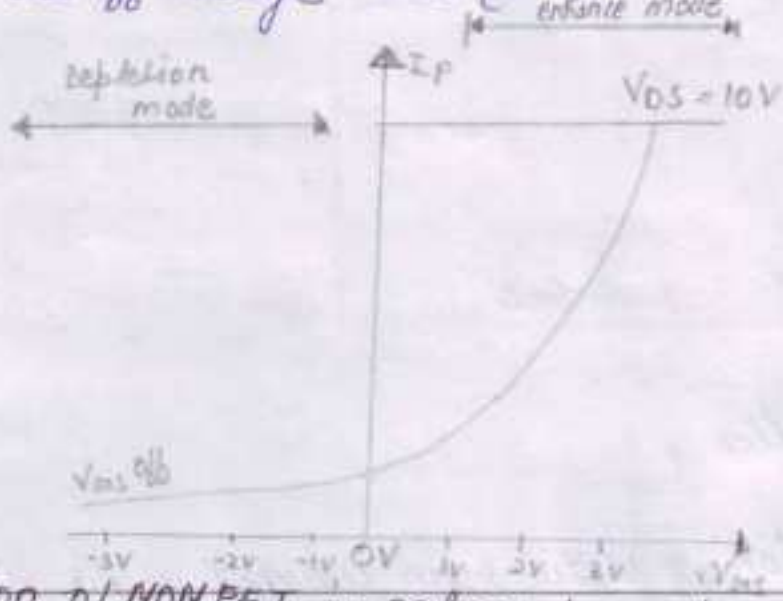
keeping V_{GS} is constant.



Transfer characteristic

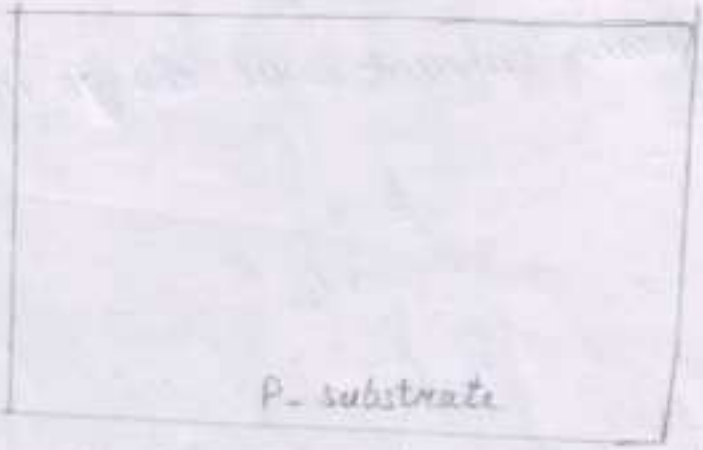
The transfer characteristics reveals that the drain current is

The gate to source voltage at which the drain current falls to an appreciably low value at recommended V_{DS} is called gate source, Cut off voltage $V_{GS(OFF)}$



Construction of NMOSFET in enhanced mode

The name is so that the drain current will only increase on application of gate voltage on grounding substrate and applying +ve potential to gate, -ve charges are induced in the substrate side. The -ve charges, thus induced from the minority carriers and form inversion layer thereby inducing a N-channel

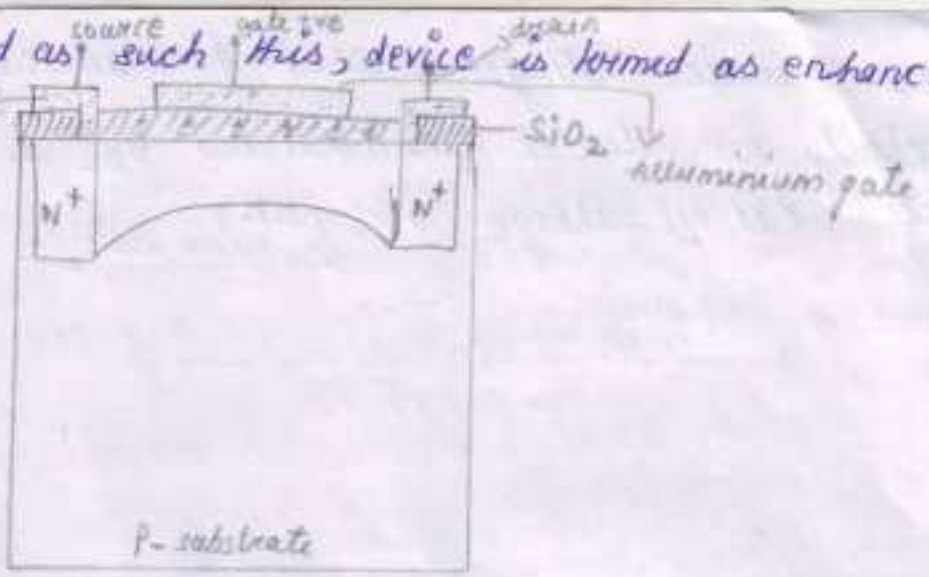


Structure of N-channel enhancement MOFEST

Working

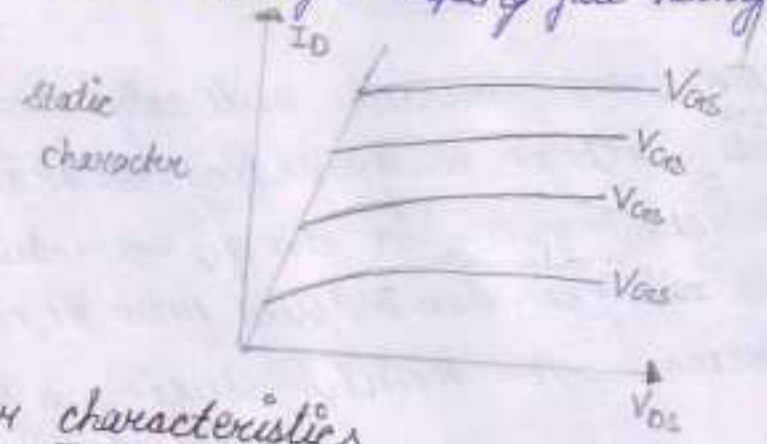
As the +ve voltage on gate increases, the -ve charges in the semiconductor increases in the channel and its conductivity increases. for a constant voltage V_{DS}, the current flowing from drain to source increases as the

gate potential and as such this, device is termed as enhanced MOSFET.



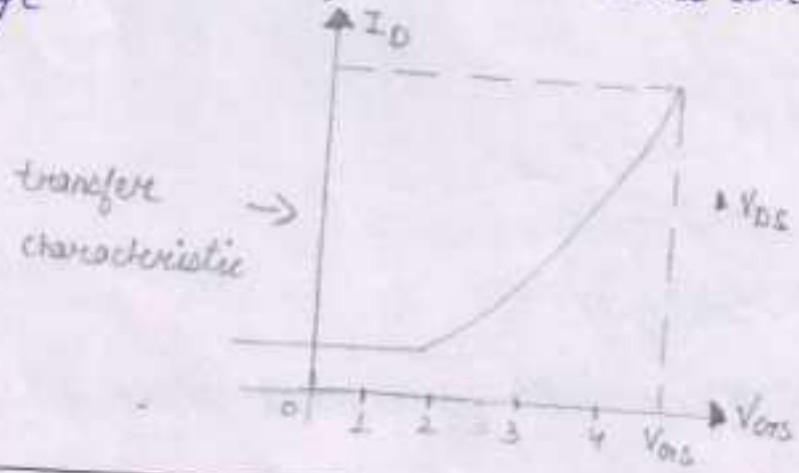
Static characteristics

It shows the variation of static drain current w.r.t change in drain to source voltage keping gate voltage constant.



Transfer characteristics

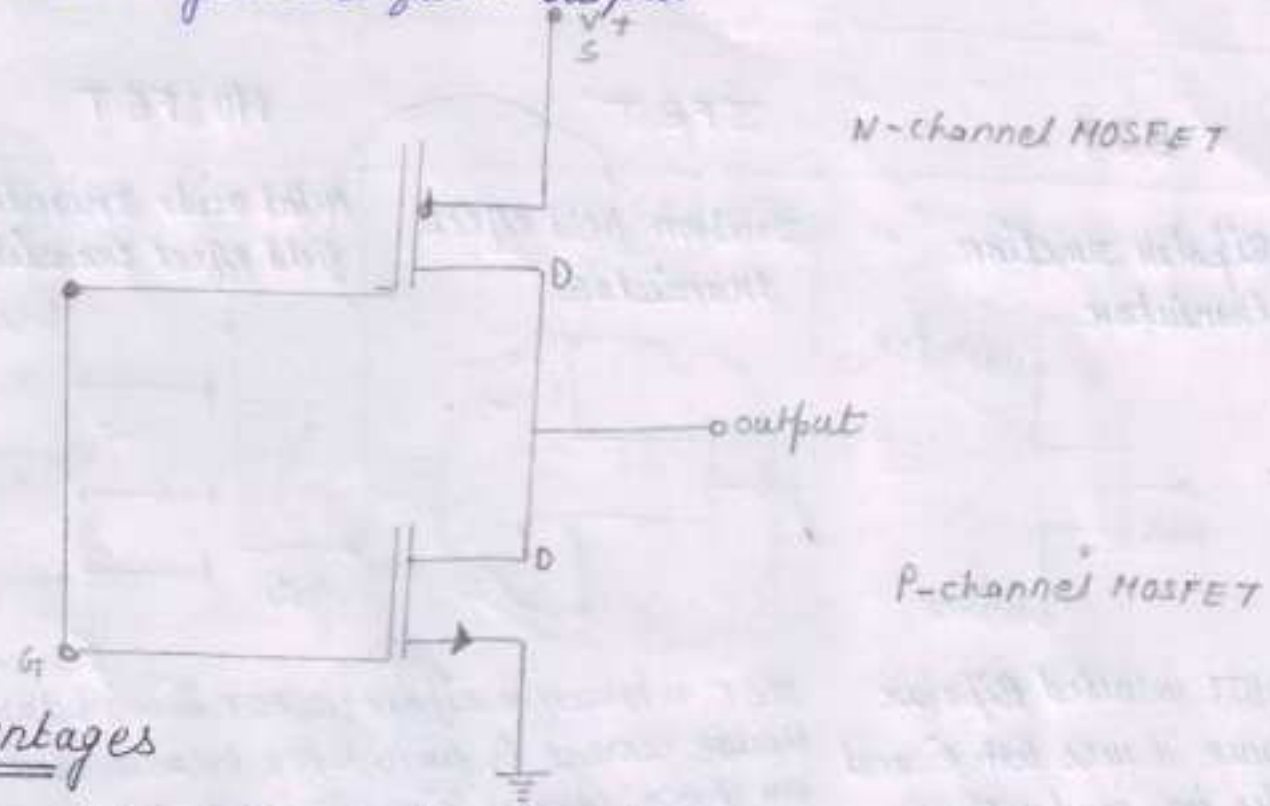
It shows variation of drain current w.r.t change in gate voltage.



CMOS

Another type of MOSFET exists, that uses complementry pairs of PMOS and NMOS.

CMOS are fabricated by making both PMOS and NMOS transistors on the same chip with common substrate. The gate contacts of both transistors are connected together, both the Drain are connected together to form output.



Advantages

i) CMOS devices have high noise immunity and low static power consumption

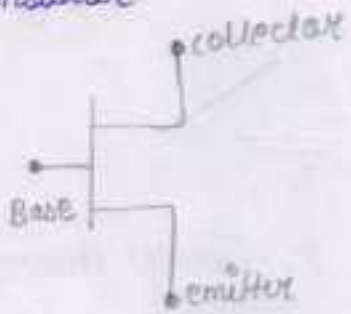
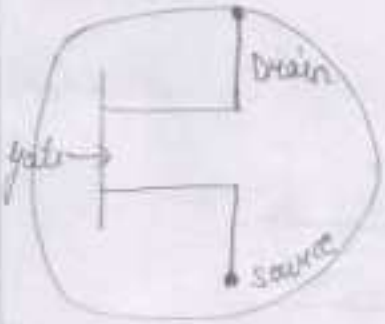
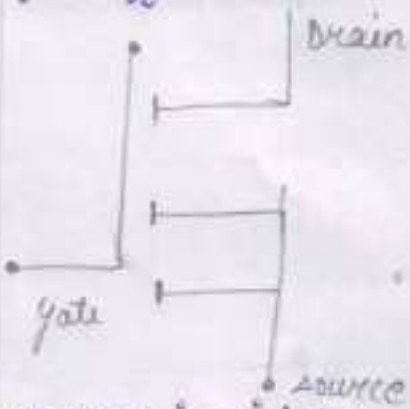
2) CMOS devices do not produce as much waste heat or other forms of logic.

iii) CMOS also allows a high density of logic functions on a chip

Application

* Recent advances in deep submicron CMOS technologies and improved pixel designs have enables CMOS based imagers to surpass charged coupled devices (CCD) imaging technology for mainstream application.
* CMOS technology is also used in analog application
* CMOS technology is used in microprocessors, microcontrollers, static RAM and other digital logic circuits

Comparison between JFET, MOSFET, BJT

BJT	JFET	MOSFET
i) Bipolar junction transistor	Junction field effect transistor	Metal oxide semiconductor field effect transistor
ii) 		
iii) BJT is called Bipolar because it uses both e⁻ and holes for conduction.	JFET is known as unipolar because current is due to one charge carrier (e⁻ or holes)	MOSFET is unipolar device because carrier is due to one charge carrier (e⁻ or holes)
iv) BJT offers low i/p resistance	iv) JFET offers large i/p resistence	MOSFET offers very large i/p resistence
v) It consist of 3 terminals like emmiter, collector, base	It consist of also 3 terminals :- gate, drain source	MOSFET consist of also 3 terminals : gate, drain, source
vi) It is current controlled devices	vi) It is voltage controlling devices	It is also voltage controlling device
vii) i/p operating region :- active, saturation, cut off	vii) operating region :- ohmic and pinch off region	Line and saturation region
viii) There is thermal run away occours at high temperature.	viii) No thermal run away.	viii) No thermal run away.
ix) fixed bias, collector bias and voltage divider baising used.	ix) self bias and voltage divider biasing used.	ix) DNOMOSFET self bias, voltage divider biasing E MOSFET :- feedback bias, voltage divider biasing
x) Input current in milliampere	x) i/p current in nano-ampere	x) gate current in picoampere
xi) used in low current	xi) used in low voltage application	xi) Since power consumption