Lesson Plan

Name of the Faculty member: Sh. Vipul Pant

Discipline: Computer Engg.

Semester: 3rd

Subject: Digital Electronics

Lesson Plan duration: w.e.f. 2nd July-16th Nov, 2018 (tentative)

Week	Theory		Practical	
	Lecture day	**Topic Covered (Including Assessment and Sessionals)**	**Practical day**	**Topic Covered (Including Viva-Voce)**
1st	1.	Introduction to Digital Electronics, Analog signals, Digital Signals	1.	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates (Gr-A)
	2.	Distinction b/w Analog & Digital Signals	2.	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates (Gr-B)
	3.	Applications and advantages of Digital Signals		
2nd	4.	Number System: Binary, Octal, Decimal & Hexadecimal, Conversion exercises	3.	Same Practical Repeated (Gr-A)
	5.	Conversion exercises on fractional numbers	4.	Same Practical Repeated (Gr-B)
	6.	Binary addition & subtraction. Subtraction using 1's & 2's Complement method		
3rd	7.	Revision of 1st & 2nd Unit	5.	Realization of Logic Functions with the help of NAND & NOR gates (Gr-A)
	8.	Codes and Parity: Concept of code, Weighted & Non weighted code, eg. BCD	6.	Realization of Logic Functions with the help of NAND & NOR gates (Gr-B)
	9.	Excess-3 code, Gray code, conversion from binary to Gray code and vice versa		
4th	10.	Concept of Parity- Single and Double parity	7.	To design a half adder using a NAND & XOR gates and verification of its operations (Gr-A)
	11.	Error Detection using Single parity	8.	To design a half adder using a NAND & XOR gates and verification of its operations (Gr-B)
	12.	Logic Gates and Families: Introduction to Logic Gates,		

		Negative and Positive logic		
5th	13.	Definitions, Symbols & Truth tables of NOT, AND, OR, NAND & NOR gates	9.	Construction of a full adder using a NAND & XOR gates and verification of its operations (Gr-A)
	14.	Definitions, Symbols & Truth tables of EX-OR & EX-NOR gates	10.	Construction of a full adder using a NAND & XOR gates and verification of its operations (Gr-B)
	15.	NAND & NOR gates as Universal gates		
6th	16.	Introduction to TTL & CMOS logic families	11.	Repetition of Practical's for Those who came Late (Gr-A)
	17.	Revision of 3rd & 4th Unit	12.	Repetition of Practical's for Those who came Late (Gr-B)
	18.	Logic Simplification: Boolean algebra-Postulates, Laws and Theorems of Boolean algebra		
7th	19.	De Morgan's Theorem with truth table, implementation of Boolean equation with gates	13.	Lab Performance & Viva-Voce (Gr-A)
	20.	Karnaugh map(K-map) upto 4-variables in developing simple combinational logic circuits	14.	Lab Performance & Viva-Voce (Gr-B)
	21.	Exercise on K-map		
8th	22.	**1st sessional Test**	15.	Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-A)
	23.	Arithmetic Circuits: Half Adder & Full Adder Circuit- Design and Implementation	16.	Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-B)
	24.	4- bit Parallel binary adder design		
9th	25.	Decoder: Introduction & 4-bit decoder circuit for seven segment display	17.	Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-A)
	26.	Multiplexer: Introduction, basic functions and block diagrams with different IC's	18.	Verification of Truth Table for Encoder & Decoder IC's, MUX and DeMUX (Gr-B)
	27.	De multiplexer : Introduction, basic functions and block diagrams with different IC's		
10th	28.	Encoder: Introduction, basic functions and block diagrams with different IC's	19.	Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-A)
	29.	Revision of 5th, 6th, and 7th Unit	20.	Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-B)
	30.	Latches and Flip Flops: Concept of a Latch, types, working & applications		
11th	31.	Flip Flop- Introduction, Defn, types RS, D,JK, T AND Master Slave Flip Flop	21.	Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-A)
	32.	Explanation of their working with truth table and wave form diagram	22.	Verification of Truth Table for Positive edge triggered & Negative edge triggered, level triggered IC Flip Flops (Gr-B)
	33.	Applications of Flip Flops,		

		Difference b/w Latch & Flip Flop		
12th	34.	Counters: Definition,Types-Synchronous and Asynchronous Counters, Their Difference	23.	To design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-A)
	35.	Binary counters: Explanation with truth Table and diagram, 2-bit, 3-bit counters	24.	o design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-B)
	36.	Mod-N or Divide by N counters: Examples with truth Table and diagram		
13th	37.	Decade Counter(both Synchronous & Asynchronous): Design	25.	To design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-A)
	38.	Up/Down Asynchronous and Synchronous Counters	26.	o design a 4-bit SISO, SIPO, PISO, PIPO shift registers using JK/D Flip Flops & verification of their operations (Gr-B)
	39.	Ring Counter and Johnson Counter		
14th	40.	**2nd Sessional Test**	27.	Lab Performance & Viva-Voce (Gr-A)
	41.	Discussion on II- sessional	28.	Lab Performance & Viva-Voce (Gr-B)
	42.	Shift Register: Introduction & basic Concept of shifting Left and Right, Types		
15th	43.	SISO, SIPO: Explanation with block diagram & Truth Table	29.	To design a 4-bit Ring Counter and verify its operations(Gr-A)
	44.	PISO & PIPO: Explanation with block diagram & Truth Table	30.	To design a 4-bit Ring Counter and verify its operations(Gr-B)
	45.	Universal Shift Register		
16th	46.	A/D & D/A Converters: Introduction & working Principle	31.	To design a 4-bit Ring Counter and verify its operations(Gr-A)
	47.	Different Techniques of A/D conversion & Study of Stair Step Ramp A/D converter	32.	To design a 4-bit Ring Counter and verify its operations(Gr-B)
	48.	Study of Dual Slope and Successive Approximation A/D converter		
17th	49.	Detail study of Binary Weighted D/A converter	33.	Use of Asynchronous Counter IC'S (7490 OR 7493) (Gr-A)
	50.	Detail Study of R/2R Ladder D/A converter	34.	Use of Asynchronous Counter IC'S (7490 OR 7493) (Gr-B)
	51.	Applications of A/D & D/A converter		
18th	52.	Semiconductor memories : Memory Organization, Classification of Semiconductor memories	35.	Lab Performance & Viva-Voce (Gr-A)
	53.	RAM: DDRAM, SRAM, ROM: PROM, EPROM,EEPROM	36.	Lab Performance & Viva-Voce (Gr-B)
	54.	Introduction to 74181 IC		
	55.	**3rd Sessional Test**		