## NAME OF THE FACULTY

: Vikramaditya

: ECE

DISCIPLINE

- : 3rd SEMESTER
- SUBJECT
- : DIGITAL ELECTRONICS

LESSON PLAN DURATION

: - 15 weeks (from July- 2018 to Dec- 2018)

WORK LOAD (LECTURE/PRACTICAL) PER WEEK (IN HOURS):- LECTURE-03, PRACTIACL-03 PER GROUP

		THEORY	PRACTICAL		
WEEK	Lecture / Hrs	TOPIC (Including Assignment/Test)	Practical / Hrs	Experiment	
1 <sup>st</sup>	1	Introduction to Digital Electronics: Distinction between analog and digital signal.	1 2	<ul> <li>Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive</li> </ul>	
	2	Applications and advantages of digital signals.	3	OR (EXOR) and Exclusive NOR(EXNOR) gates	
	3	Number System: Binary, octal and hexadecimal number system		-	
	4	Conversion from decimal and hexadecimal to binary and vice-versa.	1	C Realisation of logic functions with the help of NAND or NOR	
2 <sup>nd</sup>			2		
	5	Binary addition and subtraction including binary points. 1's and 2's complement method of addition/	3	gates	
		subtraction	1		
	6	Codes and Parity: Concept of code, weighted and non-weighted codes	2	Revision Experiment Performed	
			3		
	7	Examples of 8421, BCD, excess-3 and Gray code	1	construction of a full adder	
3 <sup>rd</sup>	8	Concept of parity, single and double parity and error detection	3	circuit using XOR and NAND gates and verify its operation	
5			1		
	9	Logic Gates and Families: Concept of negative and positive logic.	2		
			3		
			1	Verification of truth table for	
4th	10	Definition, symbols and truth tables of NOT, AND, OR Gates	2	<ul> <li>positive edge triggered,</li> <li>negative edge triggered, level</li> <li>triggered IC flip-flops (At least</li> </ul>	
	11	Definition, symbols and truth tables of NAND, NOR, EXOR Gates	3	one IC each of D latch , D flip Mux and DeMux	
			1		
	12	Definition, symbols and truth tables of NAND and NOR as universal gates.	2	-	

	13	Introduction to TTL and CMOS logic families	1	<ul> <li>Verification of truth table for encoder and decoder ICs</li> </ul>
5 <sup>th</sup>	14	Assignment-1	3	
		_	1	
		Sessional Test-1	2	
	15		3	
	16	Logic Simplification: Postulates of	1	, To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using
	10	Boolean algebra, De Morgan's Theorems	2	JK/D flip flops and Asynchronous
6 <sup>th</sup>	17	Implementation of Boolean (logic) equation with gates	3	Counter ICs (7490 or 7493
Ŭ	17		1	
		Karnaugh map (upto 4 variables)	2	Powision Experiment Performed
	18		3	Revision Experiment Performed
		Simple application in developing	1	To design a 4 hit vin a sound or
	19	combinational logic circuits	2	<ul> <li>To design a 4 bit ring counter and verify its operation</li> </ul>
	20	Arithmetic circuits: Half adder and Full adder circuit	3	
7 <sup>th</sup>			1	
			2	-
	21	Half adder and Full adder circuit, design and implementation	3	
	22	Decoders, Multiplexeres, Multiplexeres and Encoder: Introduction	1	
			2	Revision Experiment Performed
8 <sup>th</sup>	23	Four bit decoder circuits for 7 segment display and decoder/driver ICs	3	
0			1	
	24	Basic functions and block diagram of MUX and DEMUX with different ICs	2	
			3	Revision Experiment Performed
	25	Basic functions and block diagram of Encoder	1	
			2	Revision Experiment Performed
	26	Latches and flip flops: Concept and types of latch with their working and applications	3	
9 <sup>th</sup>			1	
	27	Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops.	2	Revision Experiment Performed
			3	
	28	Difference between a latch and a flip flop.	1	
			2	Devision Evenening ant Derformed
10 <sup>th</sup>	29	Assignment-2	3	Revision Experiment Performed
10			1	
	30	Sessional Test-2	2	Revision Experiment Performed
			3	

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	31	Counters: Introduction	1	To design a 4 bit ring counter
11 <sup>th</sup>	32	Introduction to Asynchronous counters	3	- and verify its operation
			 1	
				To design a 4 bit ring counter
	33	Introduction to Synchronous counters	2	and verify its operation
			3	
	34	Binary counters	1	Use of Asynchronous Counter ICs (7490 or 7493)
			2	
12 <sup>th</sup>	35	Divide by N ripple counters	3	
	55		1	Use of Asynchronous Counter
	36	Decade counter, Ring counter	2	ICs (7490 or 7493)
			3	
		Shift Register: Introduction and basic	1	
	37	concepts including shift left and shift	2	-
		right. Serial in parallel out, serial in serial		Revision Experiment Performed
13 <sup>th</sup>		out		-
5	38	Parallel in serial out, parallel in parallel out. Universal shift register.	3	
		A/D and D/A Converters: Working	2	-
	39	principle of A/D and D/A converters, Stair step Ramp A/D converter, Dual Slope A/D converter.	3	– Revision Experiment Performed
	40	Successive Approximation A/D Converter, detail study of : Binary Weighted D/A converter, R/2R ladder D/A converter. Applications of A/D and D/A converter	1	-
			2	Revision Experiment Performed
14 <sup>th</sup>	41	Semiconductor Memories: Memory	 3	
		organization, classification of Semiconductor memories	1	
	42	(RAM, ROM, PROM, EPROM, EEPROM),	2	Revision Experiment Performed
		static and dynamic RAM	3	-
	43	Introduction to 74181 ALU IC	1	
			2	Revision Experiment Performed
15 <sup>th</sup>	44	Assignment- 3	3	
10			1	
	45	Sessional Test- 3	2	Revision Experiment Performed
			3	